**Abstract**

The large mismatches among the coefficients of thermal expansion (CTE) of the metal via, insulator liner, and Si substrate of the through-silicon via (TSV) induce thermal stresses within and around the TSV during thermal-cycled fabrication processes. Reduction of thermal stress in the Si substrate is important for minimizing the deviations in the device characteristics. An annular-trench-isolated (ATI) structure was proposed for the TSV to solve the thermal issues, which occur during the three-dimensional (3D) integrated circuit (IC) integration, by stress redistribution. The concept of ATI TSV is based on retaining a Si-ring between the metal core and insulator layer during the fabrication process. We realized the ATI TSV using a via-last fabrication approach, with two deep silicon etching processes (Bosch processes) for the insulator layer and the metal core. Parylene-HT was utilized as the insulator to achieve high uniformity. With a vacuum-assisted filling system, the vias were filled with a solder material. ATI TSVs with diameters of 10 μm and 2-μm-thick Parylene-HT insulation layers were demonstrated. Studies on the thermal stress levels of the ATI TSV were carried out by finite-element method (FEM) simulation, along with comparisons with regular and annular TSVs. We revealed that the ATI TSV shows lower thermal stresses in the Si substrate than the regular and annular TSVs. The ATI TSV is a possible candidate for 3D IC integration with stress-sensitive devices