Organic low-k materials have been considered in the literature for satisfying the requirements of lowering the dielectric constant of the dielectric layer to decrease the problem of signal delay, lower power consumption, and to reduce cross talk between the neighboring paths, and lowering the fabrication temperature budget. In this paper, the feasibility of using Parylene-HT as a low-temperature deposition, high-uniformity coverage low-dielectric liner for copper-filled through-silicon vias (TSVs) in 3-D integration is investigated. In particular, the capability of embedding Parylene-HT in via-last fabrication process is validated through the demonstration of 100-μ m-depth bottom-up copper-filled TSVs. TSVs with Parylene-HT as a liner were realized through vias etching, parylene vapor deposition, and copper electroplating processes. The Parylene-HT deposition and copper electroplating processes were implemented at room temperature, such that thermal-related issue would be avoided and device reliability would be enhanced. The insulation function of the Parylene-HT liner of the fabricated TSVs was characterized. Capacitance of 0.164 pF/TSV and leakage current density of 22 pA/cm2 at a field of 0.25 MV/cm were obtained through the measurement of the TSV arrays. The obtained results reveal the possibility of using such a high potential parylene in low-temperature budget 3-D integration applications.