

Huge on-Current Ferroelectric-Gate Thin Film Transistor with Solution-Processed Indium Tin Oxide Channel

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Abstract: We have demonstrated ferroelectric-gate thin film transistors (FGTs) using solution-processed indium tin oxide (ITO) film as an oxide-semiconductor channel and $\text{Pb}_{1.2}\text{Zr}_{0.4}\text{Ti}_{0.6}\text{O}_3$ ferroelectric film as a gate insulator on a poly-crystalline 100-nm-STO/ SiO_2 /Si substrate or a single-crystalline STO(111) wafer. The FGTs show a clear memory function with an on/off current ratio of more than 10^5 and a memory window of 2 V. It is interesting that even using solution-processed ITO channel, the saturated “on” current in the FGT reached as high as 4.6 mA at operation voltages of 8 V, corresponding to a field-effect mobility of $8.0 \text{ cm}^2/\text{Vs}$, for the case of single-crystalline STO(111) wafer. The large “on” current is mainly due to the huge induced charge of the ferroelectric gate, compensated to the small mobility of the ITO channel.

Keywords: PZT, Thin film transistor (TFT), ferroelectric, ITO, FeRAM.

1. Introduction

In recent years, a ferroelectric-gate thin film transistor (FGT) using an oxide-semiconductor channel and a ferroelectric-gate insulator has attracted considerable interests because of the advanced device functions such as high-density integration, nondestructive readout operation and high nonvolatile data storage. For instance, zinc oxide (ZnO) [1-3], Sb-doped tin oxide ($\text{SnO}_2\text{:Sb}$) [4], and indium tin oxide (ITO) [5], have been used as an oxide-semiconductor channel of FGT, which was commonly prepared by vacuum-deposition methods such as rf magnetron sputtering and pulse laser deposition. However, vacuum-deposition methods require expensive equipments and make production cost high.

Solution-processed and low-temperature deposition (less than 500°C) methods are to be expected both to have a glass substrate compatibility and to make its fabrication process simpler for low cost

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production [6]. Recently, oxide-semiconductor channel-based thin film transistors (TFTs) have been increasingly studied for large-area flat-panel displays and system-on-panel applications. In particular, the transistor operation of TFTs with a channel layer such as (ZnO) [7,8], indium gallium zinc oxide (IGZO) [9], indium zinc oxide (IZO) [10,11], and ITO [12] has been successfully demonstrated using solution-processed and low-temperature deposition methods. However, when the gate insulator is paraelectric, TFT devices need a high-operation voltage due to a small induced charge density coming from the paraelectric materials. This drawback can be solved by introducing a ferroelectric layer for the gate insulator, which possesses an additional advantage as to have a memory function.

In this paper, we present a solution-processed ITO film crystallized at 450 °C as the oxide-semiconductor channel to fabricate the FGT with a $\text{Pb}_{1.2}\text{Zr}_{0.4}\text{Ti}_{0.6}\text{O}_3$ (PZT) ferroelectric-gate insulator. We obtained a clear memory function for the FGT, whose “on/off” current ratio is more than 10^5 , and whose memory window is 2 V. It is interesting that, even for the solution-processed ITO channel with a low carrier concentration and a low conductivity, a very large saturated “on” current of 4.6 mA was achieved at operation voltages of 8 V, which is larger than that obtained from the FGT with a sputter ITO channel [5], and solution-processed ITO channel as we reported previously [13-15].

2. Experiment

We fabricated a FGT with a bottom-gate and bottom-contact configuration, as shown in Fig. 1.

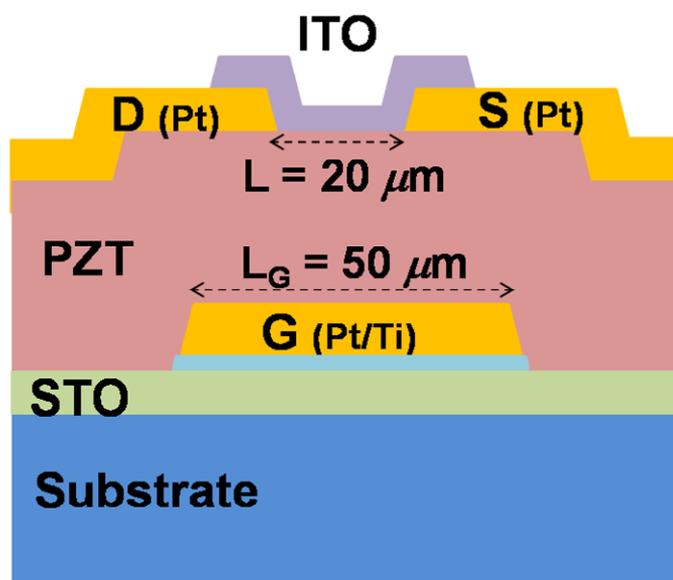


Fig. 1. Schematic drawing of the FGT with a bottom-gate and top-contact configuration.

First, a Pt/Ti (100 nm/20 nm) bottom gate was formed by sputtering on a poly-crystalline 100-nm-STO/SiO₂/Si (pc-STO/SiO₂/Si) substrate or a single-crystalline STO(111) wafer (sc-STO(111)).

Second, a 160-nm-thick PZT film having a composition of $\text{Pb}_{1.2}\text{Zr}_{0.4}\text{Ti}_{0.6}\text{O}_3$ was prepared by a sol-gel method. The PZT film was consolidated at 400 °C for 15 min, and then crystallized at 500 °C for 30 min in air atmosphere to obtain a (111)-preferred orientation. Third, a 100-nm-thick Pt film was formed as the source and the drain electrodes of the FGT by sputtering. Next, a 5%wt Sn-doped ITO precursor solution (Kojundo chemical laboratory company, Japan) was spin-coated, dried at 250 °C for 5 min, and consolidated at 400 °C for 15 min to form the ITO film. Thereafter, the ITO film channel area was isolated by reactive ion etching. The channel length (L), channel width (W) and gate length (L_G) of the fabricated FGT were 20, 60 and 50 μm , respectively. Finally, the ITO channel was crystallized in air atmosphere by using rapid thermal annealing. We found that, if the annealing temperature was higher than 450 °C, the on/off current ratio decreased because of the strong diffusion at the ITO/PZT interface and of the difficulty in depletion for the FGT with a high conductive ITO channel. Also, the off current became large due to a large gate leak from the channel area. On the other hand, if the annealing temperature was a little bit lower than 450 °C, the memory window of the FGT was narrow due to the poor crystallinity of the ITO film. As a result, the best operation of the FGT corresponded to an ITO channel annealed at 450 °C for an hour, for which the carrier concentration, resistivity and thickness were 10^{18} cm^{-3} , 0.3 Ωcm and 25 nm, respectively.

3. Results and discussion

Figure 2(a) shows the thermogravimetry and differential thermal analysis (TG-DTA) profile of the ITO precursor solution, measured by using TG-DTA8120 model, Rigaku, Japan. The first endothermic reactions with large weight losses were observed at 90 °C due to solvent evaporation. The exothermic peak at 408 °C without weight loss corresponds to the crystallization of the ITO. According to the TG-DTA result, the ITO crystallization temperature is rationalized to be around 450 °C from the viewpoint of a low-temperature process. Figure 2(b) shows a cross-section transmission electron microscope (TEM) image at the channel area of the FGT on the PZT/Pt/Ti/STO/SiO₂/Si substrate, which was observed by using H-7100 model, Hitachi, Japan. It is found that the sol-gel process ITO and PZT films were grown dense enough on the Pt bottom gate. The insert of Figure 2(b) shows a larger-scale image at the ITO/PZT interface. It is obvious that there is no serious reaction between the ITO and PZT films, which strongly supports the operation of the FGT. One notices on the FGT structure (see Figure 1) that, the ferroelectric-gate PZT layer is not only grown on the Pt bottom gate, but also on the STO film layer to isolate each FGT cell in the integration circuit. Thus, we fabricated FGTs on both a pc-STO/SiO₂/Si substrate and a sc-STO(111) wafer as a comparison of transistor operation. In this study, the PZT film was preferentially (111)-oriented on a Pt(111) film or on a sc-STO(111) wafer, and was randomly-oriented on a pc-STO/SiO₂/Si substrate, although the XRD results were not shown here.

Figure 3(a) and (b) shows polarization-applied voltage (P - V) hysteresis loops of the 160-nm-thick PZT film measured from FGTs on the pc-STO/SiO₂/Si substrate and on the sc-STO(111) wafer, respectively. For this measurement, the bottom gate was connected to the applied voltage, while the source and the drain of the FGTs were connected to the ground as seen from the insert of Figure 3.

One can observe that both P - V loops have a good squareness and symmetry. The remnant polarization (P_r) of the PZT film is $22 \mu\text{C}/\text{cm}^2$ for the FGT on the pc-STO/SiO₂/Si substrate, which is lower than the P_r of $31 \mu\text{C}/\text{cm}^2$ for the FGT on the sc-STO(111) wafer. This is because the crystalline quality of PZT and Pt films on the pc-STO/SiO₂/Si substrate is worse than that on the sc-STO(111) wafer as mentioned above.

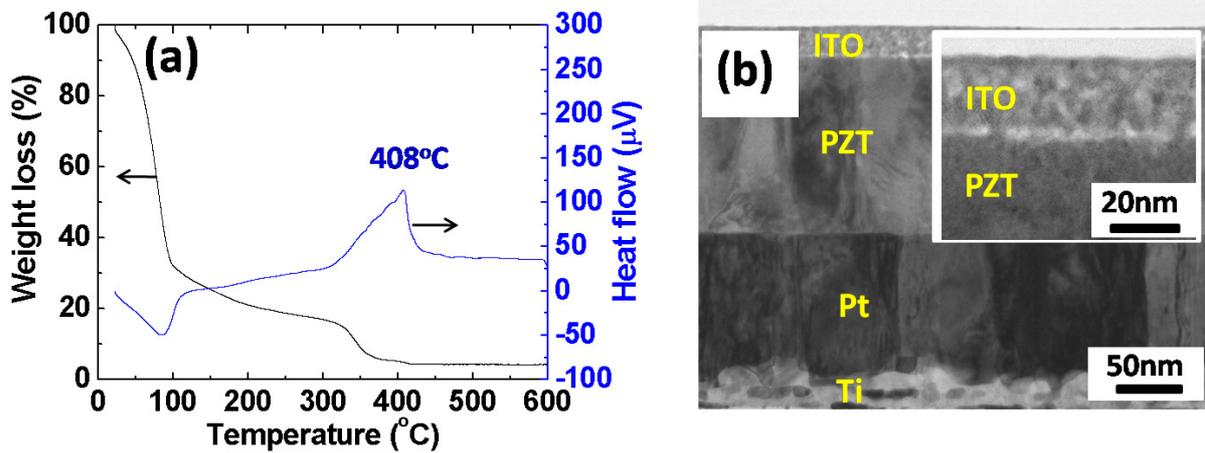


Fig. 2. (a) TG-DTA profile of the ITO precursor solution and (b) cross-section TEM image at the channel area of the FGT.



Fig. 3. Polarization-applied voltage (P - V) hysteresis loops for the FGTs fabricated on: (a) a poly-crystalline STO/SiO₂/Si substrate and (b) a single crystalline STO(111) wafer.

Figure 4(a) and (b) shows the transfer characteristics (I_D - V_G) of FGTs fabricated on the pc-STO/SiO₂/Si substrate and sc-STO(111) wafer, respectively. The gate voltage V_G was swept from -7 to

7 V and returned to -7 V at a constant drain voltage V_D of 1.5 V. The I_D - V_G curves imply a typical n-channel transistor with a counter-clockwise hysteresis loop, indicated by arrows, which exhibits a clear memory function of FGTs originating from the nature of ferroelectric materials. Here, we can estimate the memory window to be about 2 V, which is almost equal to the twice coercive voltages ($2V_c \sim 2$ V) shown in Figure 3. This is theoretically reasonable and indicates the effectiveness of the low-temperature process (450 °C) for the sol-gel ITO channel because the well-formed ITO/PZT interface causes a small trap density, and the pinning domains might be negligible at the ITO/PZT interface. Next, we can see in Fig. 4(b) that the drain current of the FGT on the sc-STO(111) wafer is saturated easily and that the I_D - V_G loop is square, which are better than those of the FGT on the pc-STO/SiO₂/Si substrate shown in Fig. 4(a). This behavior is consistent with that shown in Fig. 3, where the polarization for the FGT on the sc-STO(111) wafer is also saturated more easily, and where the P - V loop is more square. This indicates that the shape of the I_D - V_G loop is related to that of the P - V loop, i.e., the crystalline and ferroelectric quality of the PZT film is important for the FGT operation. From Fig. 4, we can also see that the on/off current ratio for the FGTs is about 10^5 and 10^6 on the pc-STO/SiO₂/Si substrate and the sc-STO(111) wafer, respectively. When $V_G < 0$, the “off” current is less than 10^{-10} A for the FGT on pc-STO/SiO₂/Si substrate and less than 10^{-8} A for the FGT on the sc-STO(111) wafer. These off currents are lower than that of the sputter-ITO channel FGT ($>10^{-8}$ A), as we reported before, even though the thickness of the sol-gel ITO film (25 nm) is thicker than that of the sputter ITO film (10 nm) [5]. We are convinced that the sol-gel ITO channel can be depleted more easily due to a lower conductivity and a lower carrier concentration, compared with the sputter ITO channel.

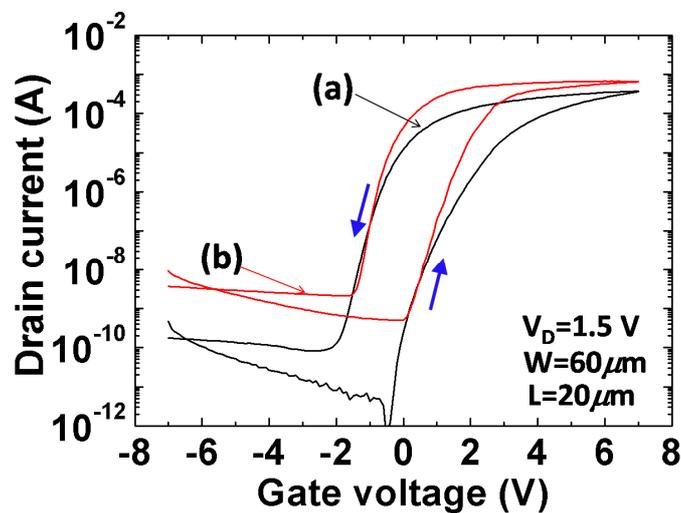


Fig. 4. Transfer characteristics of the sol-gel ITO channel FGTs fabricated on: (a) a poly-crystalline STO/SiO₂/Si substrate and (b) a single crystalline STO(111) wafer.

Figure 5(a) and (b) shows the output characteristics (I_D - V_D) of the FGTs on the pc-STO/SiO₂/Si substrate and on the sc-STO(111) wafer, respectively, which were tested by a semiconductor parametric analyzer (Agilent 4155C). The V_D was swept from 0 to 8 V, while the V_G was also increased from 0 to 8 V with a step of 1 V. It is interesting to note that a typical n-channel transistor operation with a very large “on” saturated current up to 3 and 4.6 mA was obtained when $V_G = V_D = 8$ V on the pc-STO/SiO₂/Si substrate and on the sc-STO(111) wafer, respectively. These values are larger than the I_D of 2.5 mA obtained from the FGT with a sputter ITO channel [5]. Also, it is much larger than the I_D of 0.8 mA at large operation voltages $V_G = V_D = 100$ V from the TFT with a sol-gel ITO channel and SiO₂ gate insulator as reported by Kim *et.al* [12]. Based on this work, the field-effect mobility (μ_{FE}) of the sol-gel ITO channel FGT was estimated to be 8.0 cm²/Vs for the FGT on the sc-STO(111) wafer. This μ_{FE} is a little smaller than that of the sputter ITO channel FGT, of which μ_{FE} is 9.1 cm²/Vs [5]. Also, it is comparable with other solution-processed channels, e.g. the ZnO-based TFT (<0.8 cm²/Vs), [7,8] the IGZO-based TFT (<7.9 cm²/Vs) [9], the IZO-based TFT (7.3-16.1 cm²/Vs) [10,11], and the ITO-based TFT (around 10 cm²/Vs) [12]. Furthermore, we estimate the saturated drain current per unit gate width is about 0.03 mA/ μ m at operation voltages of 5 V from this work, which is comparable to that obtained from the conventional MOSFET with the same channel length. This supports that the sol-gel ITO channel FGT is very expected to the LSI downscaling because its structure is one simple transistor and the large output signal is obtained mainly due to the huge induced charge of the ferroelectric gate compensated to the small mobility of the sol-gel ITO channel. This is different from the MOSFET, of which the on current is mainly contributed from the large mobility of the Si channel.

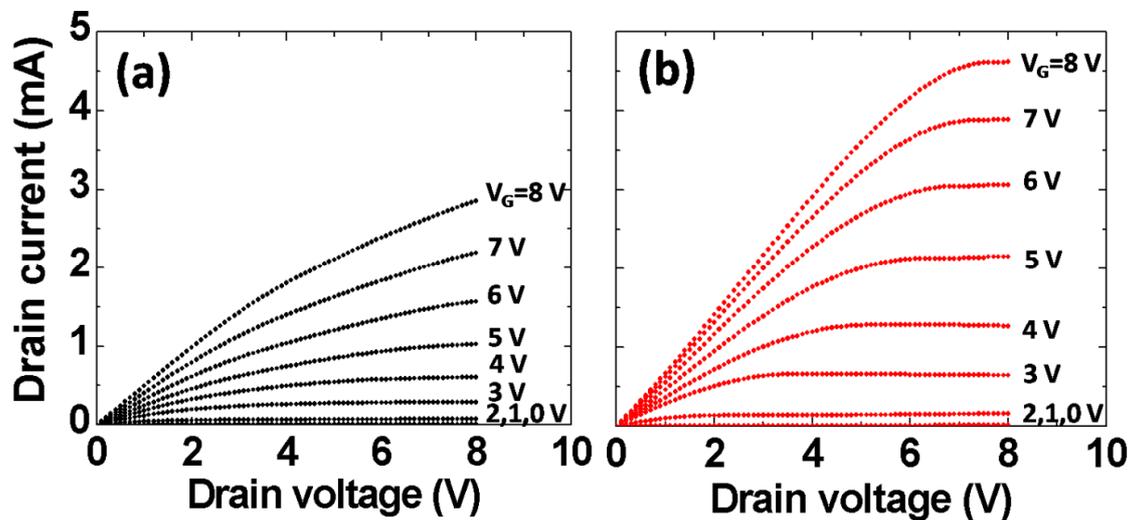


Fig. 5. Output characteristics of the sol-gel ITO channel FGTs fabricated on: (a) a poly-crystalline STO/SiO₂/Si substrate and (b) a single crystalline STO(111) wafer.

4. Conclusion

In summary, we obtained an excellent operation for the FGTs fabricated on both a pc-STO/SiO₂/Si substrate and a sc-STO(111) wafer, in which the ITO channel was prepared by a solution-processed method and annealed only at 450 °C. In particular, we demonstrated a typical n-channel FGT with a square transfer characteristic loop, whose on/off current ratio is larger than 10⁵, and whose memory window is 2 V. It is interesting that a large saturated “on” current as high as 4.6 mA can be achieved at operation voltages of 8 V. From the achievement, we believe that the FGT with a solution-processed ITO channel and PZT ferroelectric-gate insulator proposes a new challenge for the future of nonvolatile ferroelectric memory devices, which directly support to data decoding, without any amplifier.

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