# Investigation on solution-processed In-Si-O thin film transistor via spin-coating method

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In this work, we have explored optimum fabrication condition by a solution processing method for 3 at.% Si doped indium oxide thin-film transistors (TFTs). In-Si-O (ISO) thin films were investigated by X-ray reflectivity (XRR) and X-ray diffraction (XRD) techniques, and the operation of TFTs were characterized by a conventional three-probe method. XRR results suggested that as the annealing temperature increased, the film thickness decreased. In addition, according to XRD measurement, the ISO film started crystalline from 850 °C regardless the film thickness. The best ISO TFT showed the value of $V_T$ of –5 V, $\mu$ of 1.32 $cm^2$/Vs, SS of 1 V/dec, and on/off current ratio about $10^7$.

## 1. Introduction

Toward 2020 Tokyo Olympic, 8K technology has developed and conducted research by many groups. For this purpose, amorphous oxide semiconductors (AOSs), such as In-Ga-Zn-O (IGZO), have been intensively studied as channel materials of thin-film transistors (TFTs).[1-3] They are expected to take over other conventional semiconductors such as polycrystalline Si and amorphous Si. Despite the high performance of IGZO, improvement of oxygen defects and stabilization of amorphous structure are still issue to be solved.[2-5] A new AOS material called amorphous Si-doped indium oxide (In-Si-O or ISO) was developed and found that it has potential for a low-energy consumption 8K display because its structure is more stable than IGZO ones.[6-11]

Solution processing is a strong candidate for TFTs fabrication (as compared to physical vapor deposition) because of its simplicity, low cost, low power consumption, and low waste materials.[12-18] Recently, we have first reported on solution-processed ISO transistors for application of next-generation flat panel displays.[19] Nonetheless, the performance of ISO TFTs is required further improvements for the satisfactory operation. In this work, ISO TFTs were studied more details with various fabrication conditions to achieve the best performance.

## 2. Experiments

The thin-film fabrication process was similar to the work of our previous publication.[19] Firstly, indium chloride powder was dissolved in a mixed solvent, which was a compound of acetonitrile and ethylene glycol. The molar concentration of indium chloride was 0.05 M, and the volume ratio between ethylene glycol and acetonitrile was 1:50. Next, tetraethyl orthosilicate was added to the reaction solution with Si content to In of 3 at.%. Then the precursor solution was stirred to reach high degrees of uniformness and consistency.

$SiO_2$ (250 nm)/Si (high doped p-type) substrates were used in this work. The substrate was sonicated in acetone for 10 min and 1 M sodium hydroxide for 5 min. After that, the prepared precursor solution was dropped on the substrate and rotated at a speed of 3000 rpm for 30 s. The obtained sample were dried at 100 °C for 5 min, and the coating process was repeated several times to achieve a desired thickness. Finally, the samples were annealed for 1 h at various temperatures from 400 to 1000 °C in air for structural investigation, which was characterized by X-ray reflectivity (XRR) and X-ray diffraction (XRD) techniques using a Rigaku Ultima IV system. To manufacture a transistor, 200 nm-thick Al source and drain electrodes were deposited by thermal evaporation through a

stencil shadow mask with various channel sizes. TFTs characteristics (transfer and output characteristics) were measured by a Keysight B2912A system.

All transfer characteristics were measured in the saturation regime. Hence, the field-effect mobility $\mu$ can be determined as follows:

$$\mu = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2 \quad (1)$$

where $L$ is the channel length, $W$ is the channel width, $C_i$ is the capacitance per unit area of the gate insulator, $I_D$ is the drain current, and $V_{GS}$ is the gate-source voltage.[20,21]

## 3. Results and discussion

### *3.1. Thickness and crystallinity of ISO films*

XRR profiles of ISO was shown in Figure 1(a) for films fabricated by numerous spin-coating processes (2, 5, 10, and 20 times) at a wide range of annealing temperature. Based on the periods of oscillation from XRR data, the film thickness was estimated by GenX software [11,22] and plotted versus the annealing temperature and the spin-coating times (see Figure 1(b) and (c), respectively). As the annealing temperature increased, the film thickness decreased slightly. In addition, the film thickness can be controlled well by repeating the spin-coating process.

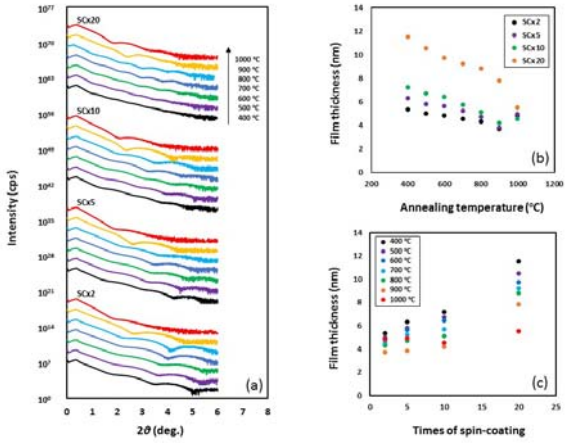


Fig. 1. (a) XRR profiles of ISO films with different spin-coating times and annealing temperature. (b) Annealing temperature and (c) spin-coating time dependence of film thickness.

Figure 2(a) illustrates the XRD profiles of ISO films at various annealing temperature. From the intensity of crystalline peaks and the estimated thickness (XRR results above), the integrated intensity and the integrated intensity per thickness at each temperature were shown in Figure 2(b) and (c), respectively. The crystalline peak appeared obviously from 850 °C, and increased significantly with the increase in annealing temperature. The higher peak intensity for more spin-coating times can attributed to the more volume of thicker films, which is consistent with XRR results. By dividing the integrated intensity to the equivalent film thickness with acceptable error bars, we can claim that the crystallinity of ISO film was independent on its thickness.

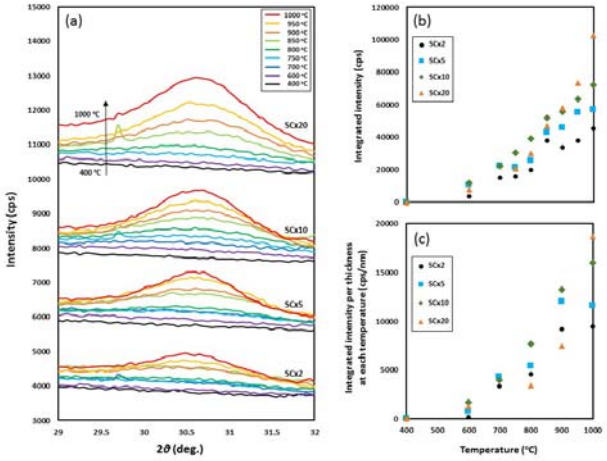


Fig. 2. (a) XRD profiles of ISO films different spin-coating times and annealing temperature Annealing temperature dependence of (b) integrated and (c) normalized peak intensity.

### *3.2. Effect of thickness on TFT characteristics*

Figure 3 describes the transfer curves of ISO TFTs for three channel lengths (*Ls*) and four film thicknesses annealed at 400 °C in air, which were obtained at the drain-source voltage $V_{DS}$ = 40 V. Among various thicknesses, the ISO film obtained at 5-time spin-coating process revealed the best mobility ($\mu$) as well as other parameters such as threshold voltage ($V_T$), subthreshold swing (SS), and on/off current ratio, was shown in Table I.

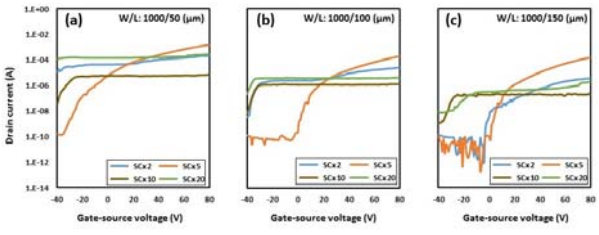


Fig. 3. Transfer characteristic of ISO films on the film thickness with 3 different channel length for various sin-coating times.

Table I. The performance of 5-time spin coated ISO TFTs annealed at 400 °C in air.

| Channel length $L$ ($\mu$m) | Threshold voltage $V_T$ (V) | Mobility $\mu$ (cm$^2$/Vs) | Subthreshold swing SS (V/dec) | On/off current ratio |
|---|---|---|---|---|
| 50 | –36 | 2.77 | 5 | $10^7$ |
| 100 | –3 | 0.92 | 2 | $10^6$ |
| 150 | –5 | 1.32 | 1 | $10^7$ |

According to the estimated film thickness in previous section, the thickness of 2-time spin coated film might be smaller than the ideal thickness of channel, while several-time one would be large. Hence, the 5-time spin-coating process would manufacture the film thickness closest to the ideal thickness of channel, leading to the best transfer characteristic among various times of spin-coating.

### *3.3. The optimized ISO TFT*

The performance of ISO TFT depended strongly on the annealing temperature. Figure 4 describes the optimized transfer (which were obtained at $V_{DS}$ = 40 V) and output characteristic of ISO TFTs annealed at 400 °C. The value of $V_T$, $\mu$, SS, and on/off current ratio were –5 V, 1.32 cm$^2$/Vs, 1 V/dec, and $10^7$, respectively. At low $V_{DS}$ region, the magnitude of drain current increased almost linearly with a slightly concave feature, suggesting the existence of a small injection barrier between the source electrodes and the channel of ISO thin films. Further studies are necessary to improve the value of $\mu$ for the satisfactory operation.

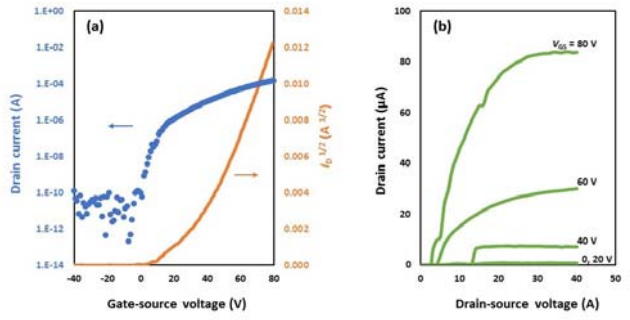


Fig. 4. The transfer and output characteristic of the optimal ISO TFTs.

## 4. Conclusions

In this report, 3 at.% Si doped indium oxide thin films were manufactured by the spin-coating technique and deeper investigated compared to the previous work. As the increasing of annealing temperature, the film thickness decreased and the crystalline peak appeared clearly from 850 °C regardless the film thickness. The best ISO TFT showed the value of $V_T$, $\mu$, SS, and on/off current ratio were –5 V, 1.32 cm$^2$/Vs, 1 V/dec, and $10^7$, respectively. Further improvement will be conducted to enhance the performance of solution-processed ISO TFTs.

**Acknowledgments**

This work was partially supported by the Hyogo Overseas Research Network (HORN) Program, Hyogo Earthquake Memorial 21st Century Research Institute, and Grants-in-Aid for Scientific Research (grant No. JP15H03568). Bui Nguyen Quoc Trinh would like to acknowledge the support provided by the Vietnam National Foundation for Science and Technology Development (NAFOSTED; grant No. 103.02-2012.81).

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