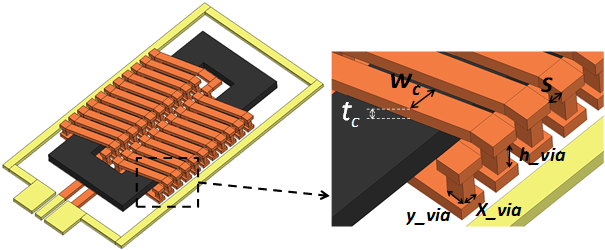
Technical Report:

Integrated inductor fabrication by monolithic approach



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# Abstract

This technical report will present the experimental approaches and technological process to realize the ferrite-based micro-inductor. The objective is to develop a technology for fabricating integrated micro-inductors on/in silicon based on ferrite as magnetic cores. Copper is chosen for the winding as top tracks, bottom tracks and vias. Electro-deposition technology is used for copper deposition.

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# 1 Introduction

According to the monolithic integration, ferrite is screen printed inside cavities in silicon wafer and sintering them with Cu tracks underneath. The feasibility of proposed methods will be evaluated by testing and developing critical process steps. It is envisaged either to bond the two levels of windings by flip chip with the core in between or to finish copper windings with photo-resist mold technology.

# 2 Process development for monolithic approach

Processes and technology were developed in the clean room at LAAS to realize the monolithic integration including the process of etching cavity in silicon wafer and the tests of co-sintering printed ferrites with the silicon wafer.

## 2.1. KOH etching and compensation for rectangular cavity

The idea to fabricate magnetic core in the first strategy is to print ferrite slurry inside the cavity in the silicon wafer where copper tracks are preliminary deposited and then sinter them. Regarding the design, the shape of ferrite core is rectangular with a hole in the middle and hence, the rectangular cavities need to be created in the silicon wafer. Heated potassium hydroxide (KOH) solutions can be used for preferential crystallographic etching of silicon. The etch rate depends on crystallographic orientation of the silicon and the concentration of KOH solution used; the temperature of KOH solution is 90°C. Normal etch rates are about 1µm/minute. However, due to the different etch rates of silicon on different crystal direction, with the normal mask of Si3N4 (see Figure 1 a)) the cavities after etching are not exactly rectangular; the inner corners are over etched (see Figure 1 b)). This is not a good shape for the rectangular core. By applying the compensation method proposed by Yu [[1](#_ENREF_6_2)], the suitable compensation was made to avoid the over etching; the well-shaped rectangular cavities are formed on silicon wafer, see Figure 2. To note in Figure 2, *D* is the depth of etching which is 200 µm in our cases (150 µm for the core and 50 µm for the bottom copper tracks). This compensation also helps avoiding a problem arising during copper tracks electroplating which is the diffraction of UV light at the over-etched corners during the process of photolithography. The angle slope is 54.7° between the surface and the plane <111> which is similar for the length direction and the width direction.

The 50 µm -thick bottom copper tracks were successfully electro-deposited on the rectangular cavities in silicon wafer, see Figure 3. The next step is to test co-sintering of silicon and printed ferrites.

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*Figure 1 : a) Rectangular mask of Si3N4 on silicon wafer b)KOH over-etched cavity in silicon wafer*

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*Figure 2 : a) Compensated mask of Si3N4 on silicon wafer and b) KOH-etched rectangular cavity in silicon wafer*

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| bot Cu on compensated KOH_m01.jpg | bot Cu on compensated KOH_m03.jpg |

*Figure 3 : Electro-deposited bottom copper tracks on rectangular KOH-etched cavity in silicon*

## 2.2. Co-sintering Si/Si3N4 wafer with printed ferrites

In order to obtain the magnetic phase of ferrite, the printed ferrite needs to be sintered at high temperature (about 900°C). In the monolithic approach, printed ferrites inside the rectangular cavities need to be sintered in the presence of silicon wafer underneath. Hence, the test was carried out to sinter the printed in-house ferrites inside the rectangular cavities in silicon wafer at 980°C during 2 hours under oxygen. After sintering, the cracks appeared at the corners and on the sides of the cores (see Figure 4). The shrinkage is roughly 27%. However, grain size is 100 - 500 nm, no big grain is formed, and this means that the ferrite is not fully sintered at 980°C like the free-standing printed in-house ferrite. In order to estimate the temperature at which ferrite is fully densified inside the cavity, we carried out TMA analysis, and the result showed a densification peak at 1030°C i.e the ferrite should be sintered at temperature about 1030°C .

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| Printed with mask 1 980C 2h compensate KOH_m02.jpg | Printed with mask 1 980C 2h compensate KOH_m09.jpg |

*Figure 4 : SEM images of in-house printed ferrite in rectangular cavities after sintering at 980° during 2 hours*

As the sintering step involves high temperature, the issue that could arise is inter-diffusion of elements between the ferrite layer and the substrate. A barrier layer (silicon nitride Si3N4) was grown by low pressure chemical vapor deposition method (LPCVD) on the substrate to avoid metal elements to diffuse into the silicon. The final stack is Si/SiOxNy (150 nm) / Si3N4 (40 nm)/ferrite U70 (24-66 µm). Interfaces were observed and analyzed with EDS SEM at LAAS and TEMSCAN service at Toulouse Paul Sabatier University. There is no silicon diffusing into the ferrite part and there is neither metal atom diffusing into the silicon substrate. No diffusion was observed for two times of examining. However, the oxidation and diffusion problems appeared when we co-sintered the copper tracks with silicon substrate underneath at 980°C during 2 hours under air condition. The copper tracks were oxidized and diffused over the surface of silicon wafer.

# 3 Conclusions and recommendations

From these experiments, we see that it is unfeasible to sinter ferrite directly on silicon, with the presence of copper windings, at that high temperature due to the problems of delamination and cracking and the problem of oxidation and diffusion. The hybrid approach should be considered .

# 4 Acknowledgements

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# 5 References

[1] J.-C. Yu, "Convex corner compensation for a compact seismic mass with high aspect ratio using anisotropic wet etching of (100) silicon", *Design, Test, Integration and Packaging of MEMS/MOEMS Symposium (DTIP 2011) IEEE*, 197 - 199, 2011