High gain low-noise amplifier design used for RF front end application

Tran Van Hoi[1] Bach Gia Duong[2]
[1]Broadcasting College 1, VOV, 136th Quy Luu, Phu Ly, Ha Nam, Viet Nam
[2]University of Engineering and Technology, VNU, 144th Xuan Thuy, Cau Giay, Hanoi
E-mail: [1]tranvanhoi@vov. org.vn, [2]duongbg@vnu.edu.vn

Abstract

This paper presents the design and fabrication of a high gain low noise amplifier (LNA) at C-band, which suitable for RF front end application. In this paper, we propose using a diagram of the two-stage cascade amplifier with different center frequency in order to create a good wide band performance and high gain. The paper also proposes using negative feedback circuit to reduce the noise figure. The LNA has been fabricated on a PCB board with FR4 substrate using microstrip technology and pHEMT FET transistor amplifier with following specifications: Maximum overall gain of 26.046dB, operating frequency from 4GHz to 5GHz, noise figure is less than 1dB, the reverse isolation of -29.5dB, the LNA using a 5V supply voltage respectively and total current consumptions of 20mA.

Introduction

To amplify the very small received signals in receiver systems, a low noise amplifier, which is placed right after the antenna, is required. Due to the signal to noise ratio in the receiver has the dominant effect of the noise of the first amplifier stage. Therefore, the goal of the designer is to design the LNA with gain as high as possible, the lowest noise figure and required wide band. In order to obtain the demand on the system consisting of the gain, noise figure, bandwidth, we have to deal with the design of two-stage LNA. The first stage will optimize the noise figure by using negative feedback circuit, and the second stage will increase an overall gain.

Design of the LNA

The configuration of the LNA in the paper is a two-stage cascade amplifier based on the design of single-stage one. The block diagram of two-stage cascade LNA is illustrated in the Fig.1. In order to achieve bandwidth 1GHz, the center frequency of the first stage is selected at 4.4GHz and at 4.6 GHz for the second stage.

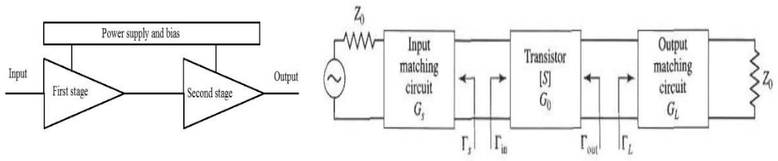

Figure 1: Two-stages cascade LNA Diagram and a single stage LNA Diagram

The completed LNA with two-stage was shown in Fig.2.

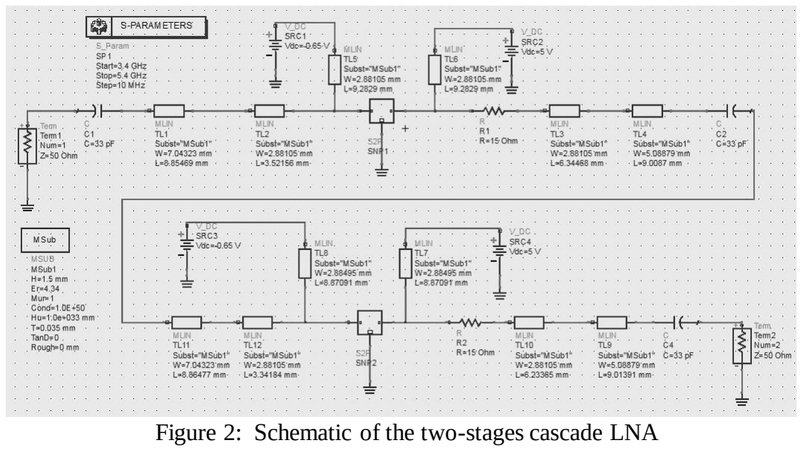

Figure 2: Schematic of the two-stages cascade LNA

Simulated Results

The initial simulations to test the LNA performance were done with the s-parameter file of the transistor. The results were shown in the bellow figs.

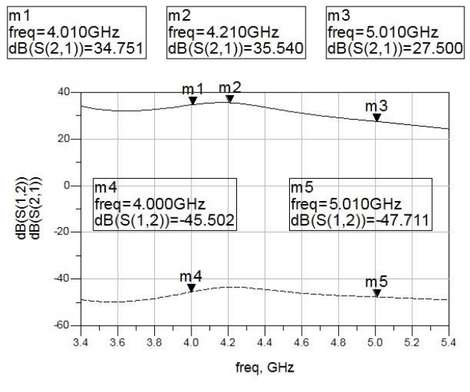

Figure 3: The S21 and S12 of the LNA

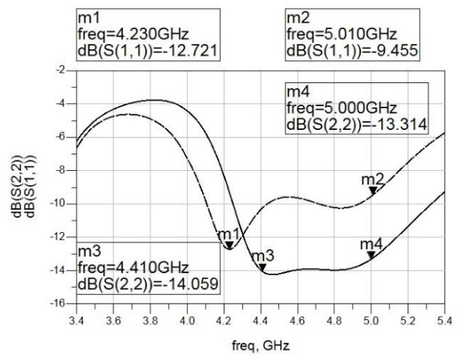

Figure 4: The S11 and S22 of the LNA

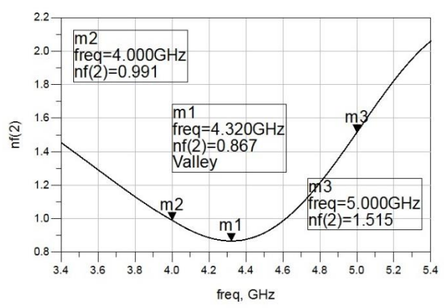

Figure 5: The noise figure of the LNA

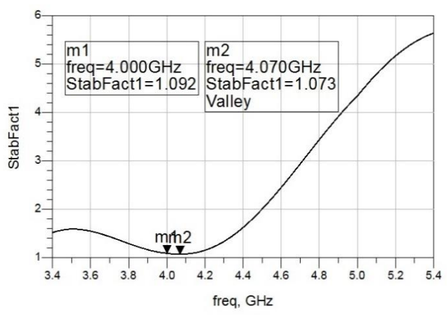

Figure 6: The stability factor of the LNA

Experimental Results

The LNA circuit was fabricated in Laboratory with the aid of the ADS package and machine LPKF Promomat C40. The testing results visually are measured on the vector network analyzer 37369D - Anritsu technology up to 40GHz.

Figure 7: The gain of the LNA

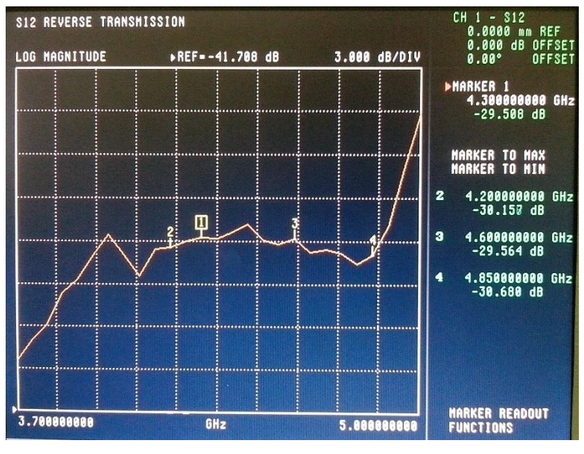

Figure 8: The S12 parameter

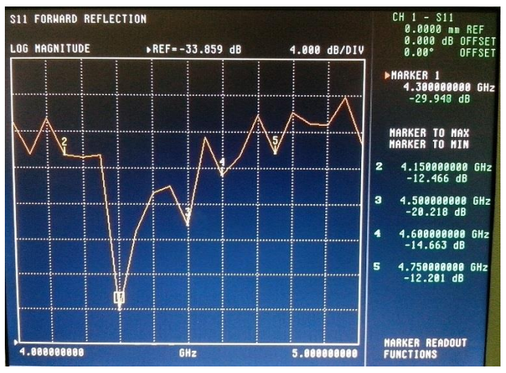

Figure 9: The input reflection coefficient

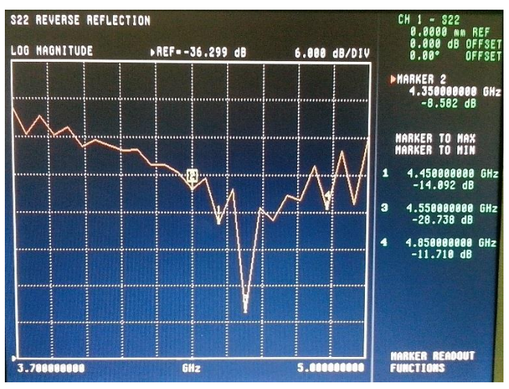

Figure 10: The output reflection coefficient

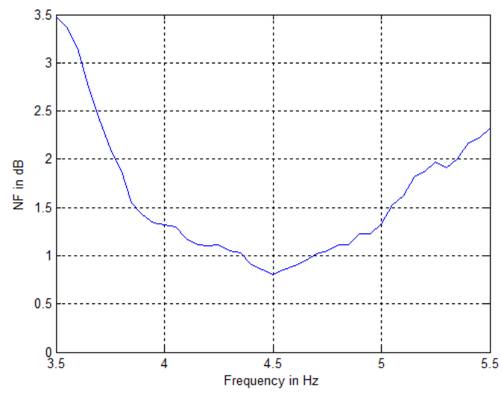

Figure 11: Noise Figure Measurement

Conclusion

A two-stage LNA with spf-3043 is designed and demonstrated with simulations in ADS package as well as tuning for the optimum gain, noise figure and bandwidth. The design was fabricated, and the board was measured and analyzed together with the simulated results. In summary, the measurement results of the LNA were compared to references with following parameters:

Parameters	This work	Ref. [1]
Frequency range	4 - 5GHz	5.1 - 5.8GHz
NF	1.20 dB	1.30 dB
S_{21}	26.046 dB	18.5 dB
S_{12}	- 29 dB	-27.3 dB
S_{11}	- 12 dB	-11.5 dB
S_{22}	- 11.7 dB	-12.3 dB

References

1. Othman A.R, Ibrahim A.B, Husain M.N, Ahmad M.T, “High Gain Low Noise Cascode LNA Using T-Matching Network for Wireless Applications”, IEEE Asia-Pacific Conference on Applied Electromagnetics (APACE 2012), 2012, pp.383-387.

2. Zhihong Dai; Yongzhong Hu; Kunzhi Xu, “Two-stage Low Noise Amplifier for BD-II Receiver Application”, 5th Global Symposium on Millimeter Waves (GSMM 2012), 2012, pp.303-306.

3. A. Abhimanyu, P. Aswathy, D. Athira, G. Gayathry, Design Of Low Noise Amplifier At 4 Ghz, International Conference on Information and Electronics Engineering, 2011, pp 209 – 212.