University of Engineering and Technology

# Sub-100nm Ferroelectric-gate Thin Film Transistor Fabricated by Two-patterning Method

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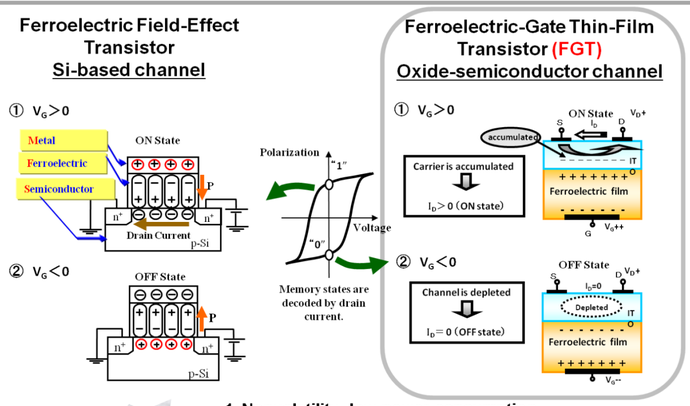
## Operational Principle

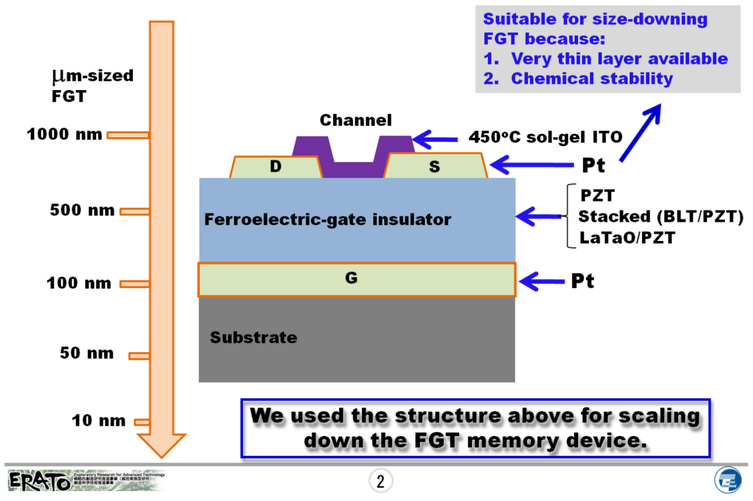



**Advantages**

1. Nonvolatility, low power consumption.
2. High operation speed.
3. High packing density and flexible substrate.



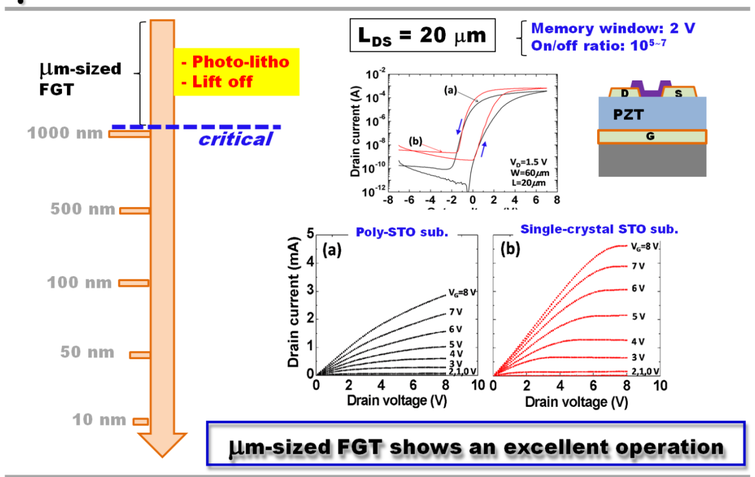
## Size-downing tendency




**We used the structure above for scaling down the FGT memory device.**



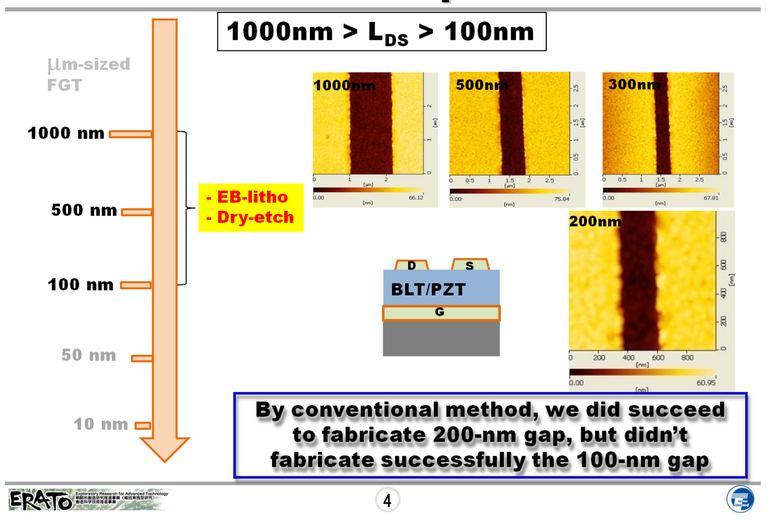
## μm-sized FGT




**μm-sized FGT shows an excellent operation**



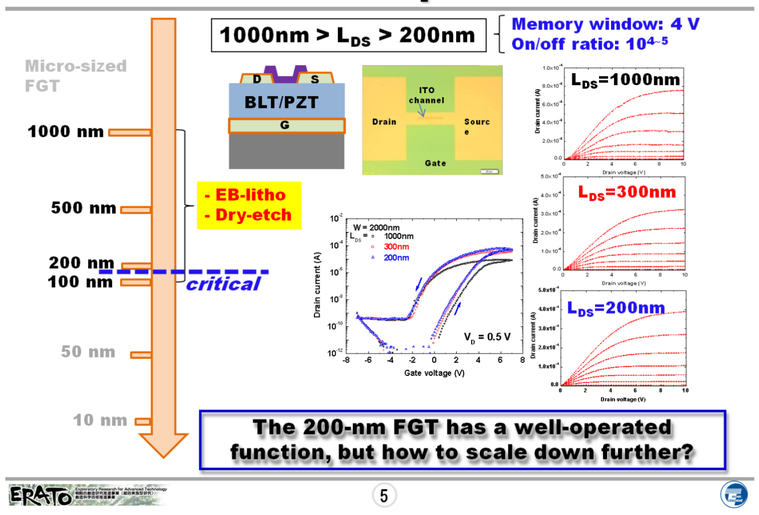
## Sub-1000nm FGTs: Gap formation




**By conventional method, we did succeed to fabricate 200-nm gap, but didn't fabricate successfully the 100-nm gap**



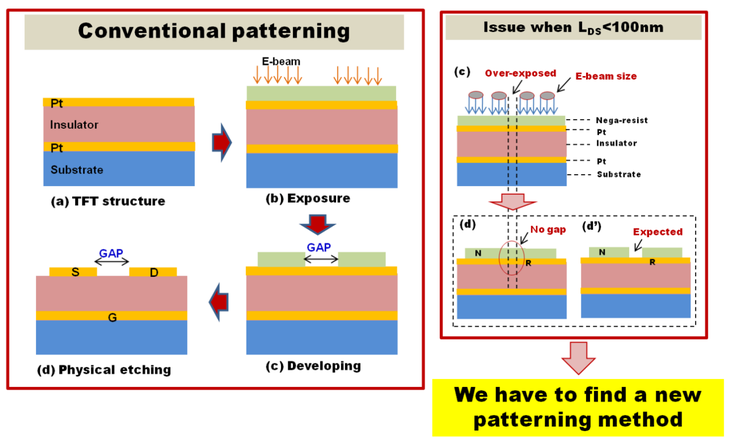
## Sub-1000nm FGTs: Operation




**The 200-nm FGT has a well-operated function, but how to scale down further?**



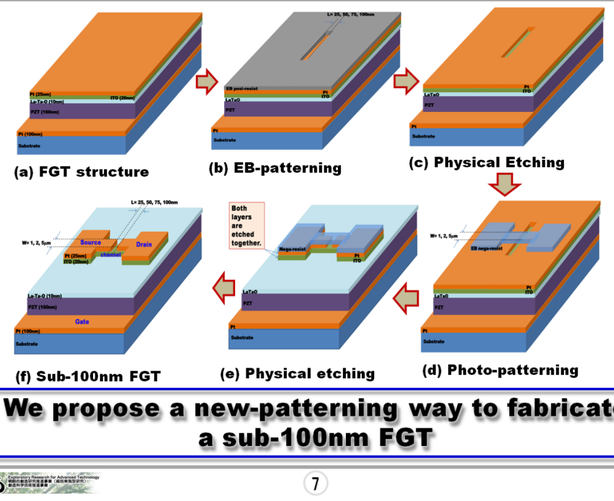
## Issues on Sub-1000nm FGTs




**We have to find a new patterning method**



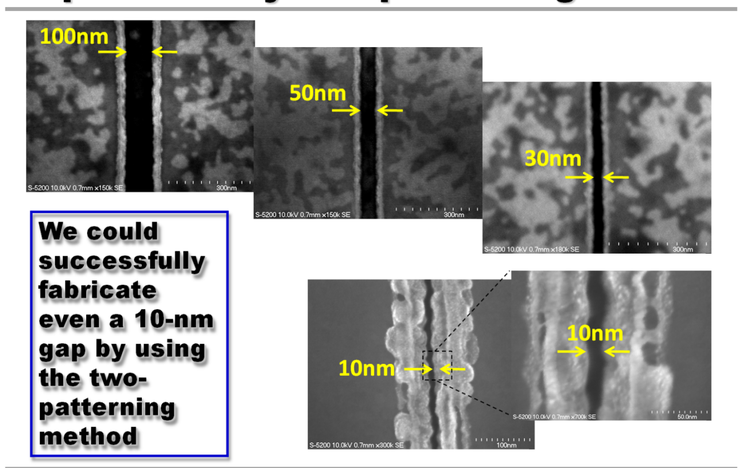
## Two-patterning method




**We propose a new-patterning way to fabricate a sub-100nm FGT**



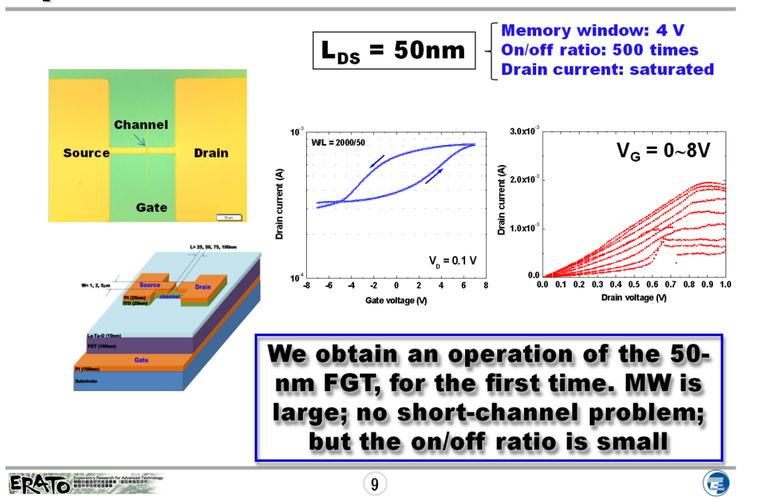
## Gap formed by two-patterning method




**We could successfully fabricate even a 10-nm gap by using the two-patterning method**



## Operation of 50-nm FGT




**We obtain an operation of the 50-nm FGT, for the first time. MW is large; no short-channel problem; but the on/off ratio is small**



## Short notes:

1. We propose a new-patterning way (so-called a two-patterning method) to fabricate sub-100nm FGTs. Up-to-10nm FGT gap could be successfully created under an assistant of the dry-etching technique.
2. By using the two-patterning method, we solve essentially the difficulties from the conventional method. As a result, we demonstrate an operation of the 50-nm FGT.
3. Taking a comparison with the μm-sized and the sub-1000 nm FGTs, the on/off ratio of the sub-100 nm FGT is much smaller. Therefore, further work should be carried out to improve and demonstrate a FGT with a size downed to 10 nm.

**Acknowledgement**

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***Thank you for a visit!***