A simple diagram for data transmission using Manchester code

Trinh Anh Vu
Faculty of Electronics and Telecommunications
VNU University of Engineering and Technology, Hanoi, Vietnam
e-mail: anhvutrinh1811@gmail.com

Pham Van Thanh
Faculty of Automation and Technical Equipment of Fire Fighting, Prevention & Rescue
The University of Fire Fighting and Prevention, Hanoi, Vietnam
e-mail: phamvanthanh1209@gmail.com

***Abstract*— The paper proposes a simple diagram for data transmission on the frequency of 2.4GHz based on the Manchester code. Unlike the classical methods, the receiver usually performs some feedback loops to stabilize the gain to control the sampling at exact position (timing) of the symbol or to synchronize and track frequency. The proposed diagram only uses a cut-off signal to detect data directly without any feedback loops. Although it is simple, the proposed diagram still obtains high stable operation and wide input dynamic range. The experiment was tested by transmitting a 64kbit image file through an embedded FPGA system. Due to the use of Manchester code, then the cost of the proposed method depends only on the bandwidth. Furthermore, the proposed diagram is more suitable for indoor transmission applications and transmitting high-speed data by using Ultra Wide Band (UWB) pulses.**

Keywords—simple diagram; Manchester code; feedback loop; indoor transmission applications.

I. INTRODUCTION

There are some processing algorithms such as Automatic Gain Control (AGC), Timing Recovery, and Carrier Recovery [1][2] in the classical digital receiver to ensure that it operates stably and synchronizes with the incoming signal. These algorithms are using the feedback loops that the output signal is compared with a reference signal (or a level). The deviation between the output and the reference is the feedback signal to adjust input signal of the system to bring the actual output closer to the reference. For example, the input signal of the AGC is compared with a threshold value. If it is greater, the feedback loop will adjust to decrease the gain and vice versa. The Timing Recovery will control the sampling at the top of the incoming symbol. If the sampling is early, the Timing adjusts it later and inversely. Phase Lock Loop (PLL) is a key component of the Carrier Recovery that can perform both in analog and in the digital domains. The complexity of the feedback loop depends on the different specific algorithms and it always occupies most of the design resource in digital receivers.

Unlike the classical diagrams, the proposed exploits the Manchester code at the transmitter and a cut-off signal at the reciever for signal separation without any feedback loops. Therefore, the proposed diagram is simple as well as high stable and wide input dynamic range signal. The proposed diagram was designed and implemented based on FPGA chip (Virtex-4) and 2.4GHz transceiver that shown a very good results when transmitting a 64kbit-image file even the magnitude of received signal changes about 18dB. The cost of the proposed method depends only on increased of the bandwidth due to the use of Manchester code. Furthermore, the proposed diagram is more suitable for indoor transmission applications and applying to UWB signal, notably in indoor environment.

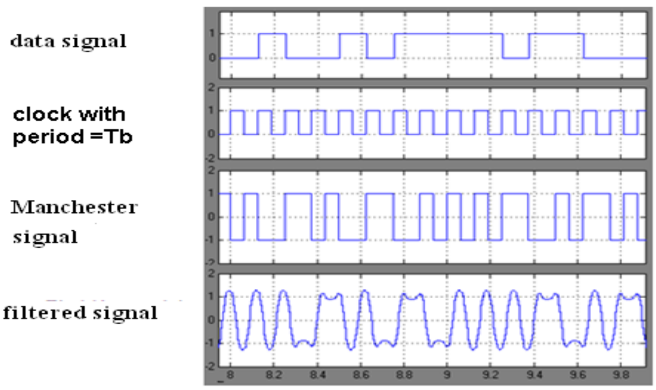
II. RELATED WORKS

II.1 Manchester code

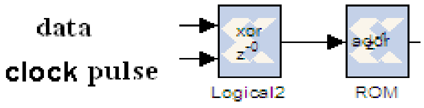
The Manchester encode and decode [5] are simply implemented by XOR operation between the binary data and the clock pulses which have a period of bit length T_b. The truth table of Manchester code [3][4] is presented as below:

original data	XOR clock	=	Manchester value
0	0		0
0	1		1
1	0		1
1	1		0
original data =	clock	XOR	Manchester value

One of the main features of the Manchester code is the pulse width that will lengthen to be double and equal to T_b when data value changes from 0 → 1 or from 1 → 0 as Figure 1a. If the data remains at the same value, the output looks like a clock pulse with a cycle of T_b and the width of ½ T_b.



a)



b)

Fig. 1. The generation of Manchester signal: a) Signal shape b) The design diagram

II.2. Design the diagram for transmitter side

Using the System Generator tool [5], we proposed a simple design as Figure 1b, where the Block ROM (Read Only Memory) will transform data from 1,0 to signal 1,-1. After ROM, the signal cannot transfer directly to the channel because the pulse has high slope and there are a lot of harmonic frequencies in signal. In fact, the signal has to be shaped after upsampling and we used a low- pass filter after upsampling 8 times as Figure 1a, then the signal is amplified and connected to the channel.

II.3. Design the diagram for receiver side

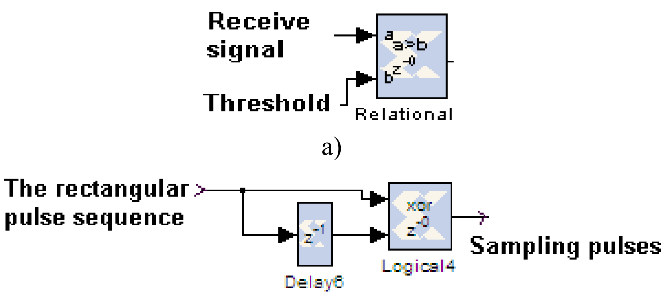
Generally, the receiver must have some units to stabilize the signal magnitude as well as control the sampling correctly at a maximum (or minimum) of the incoming signal [1]. It usually is the causes of complexity in design diagram with the feedback loops to adjust the deviation of signal from the desired position. The proposed diagram can be performed as the following steps:

- Using a threshold for cut-off signal:

A comparator in Figure 2a used to compare the received signal with a threshold V_n, (approximately 1/10 amplitude of signal). If the signal is greater than V_n, the output will be high (logic 1) and logic 0 for others. Figure 3b shows the output of the comparator after cut-off signal with a threshold that will be a rectangular pulse sequence. The length of the pulse is not the same between 1 and 0 but it always reflects the Manchester code value which carried by the signal.

- Using the XOR operator for making sampling pulses

Figure 2b shows the using XOR operator for the rectangular pulse sequence and itself, that was delayed by 1 sample after upsampled 8 times and we will get narrow pulses at the tail of the rectangular pulses. Then, these narrow pulses used for sampling the rectangular pulse sequence get value 1 for the in front of rectangular pulse, and value 0 for that behind. These values reflect exactly the value of Manchester code.



b)

Fig. 2. a) Design cutting threshold b) sampling pulses generator

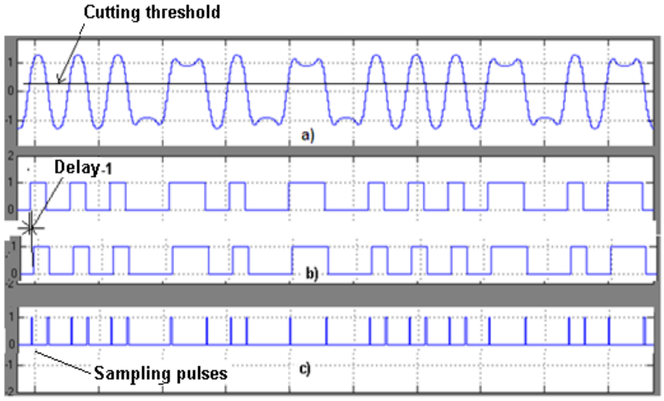


Fig. 3. Signal processing in receiver: a) input signal b) The cut-off signal by threshold c) The sampling pulses using XOR

Based on the result in Figure 3c it can be seen that:

- The average gap between the sampling pulses is Tb/2. For the threshold is greater than 0, the distance between 2 sampling pulses is closer in the positive period and further in the negative period of the incoming signal.
- If the pulse width is double, it will be lack of a sampling pulse for getting the Manchester code, this can be seen clearly when we connect the sampling pulses with reset pin of a counter. Whenever a sampling pulse comes to the reset pin, the counter will be turned into beginning or count to the maximum value (pre-determined) before returning to the start.

Figure 4 shows the output of a counter that has different peaks between positive and negative period of the received signal, and when the rectangular pulse has double length of a counter, the peak also will be double in high. Although the sampling pulses have different lengths, the sampled from the rectangular pulse sequence after the threshold always reflect exactly the peak of rectangular pulse that carried the Manchester code's information.

Two issues above can be addressed in the design diagram as follows:

Using the counter with reset pin as above for adding a sampling pulse when the rectangle impulse is double and using the FIFO to stabilize the read out data rate.

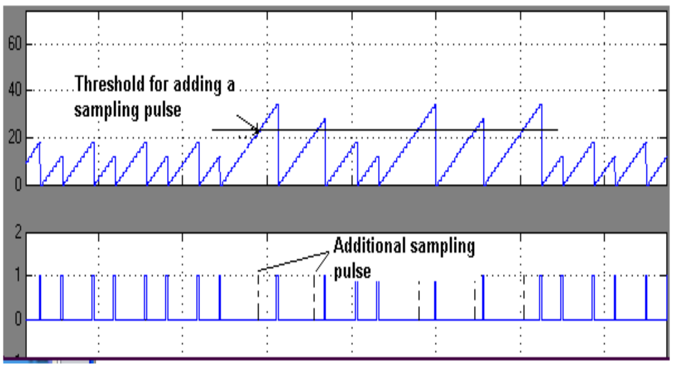


Fig. 4. The waveform of the counter output reset by sampling pulses

To add a sampling pulse where the rectangular pulses are double we used a comparator to compare the counter output with a preset value T_n (approximate to 3/4 T_b). The counter only reaches to this value when a sampling pulse is lack (or the rectangular pulse is double) and at this moment it automatically add a sampling pulses into the sampling sequence as Figure 5. Otherwise, it cannot reach to this value because it is continuous reset by sampling pulses

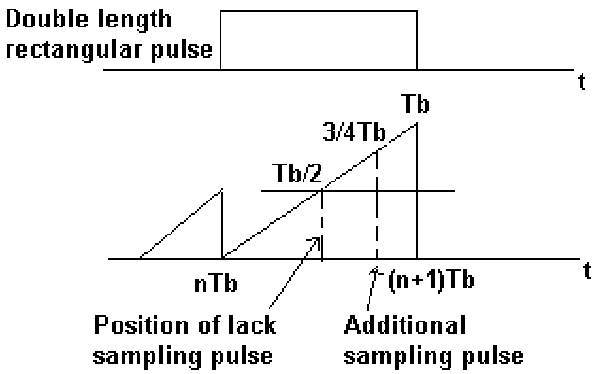


Fig. 5. Additional pulse sampling

In theory, T_n can get any values in the range of:

$$T_b/2 < T_n < T_b$$

As mentioned above, the gap between the sampling pulses fluctuate around the average value of T_b and depending on the cutting threshold V_n, we can set $T_n = 3/4T_b = 6$ (if Upsampling 8 times)

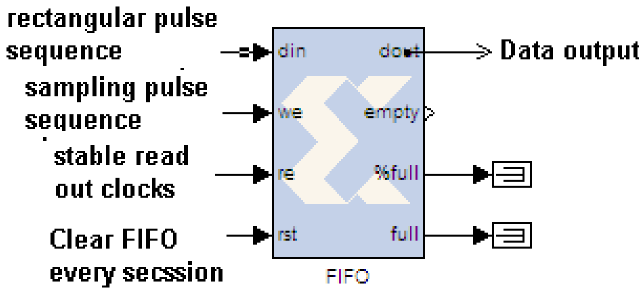


Fig. 6. The FIFO unit

Figure 6 shows the use of FIFO unit to regulate the sampling speed of signal. The writing input of FIFO (Write pin) is the sampling pulses which have non-regular speed, but the read out clock of FIFO is constant and equal $T_b/2$. In addition, the volume of FIFO is large enough for a big size of desired transmitted data. Furthermore, the difference between the primary clocks of transmitter and receiver (although very small) can lead to overflow FIFO or empty in vice versa. Moreover, the incoming signal also must have the header to reset FIFO in every session.

We emphasized the key role of the counter with reset pins in the proposed technique. It not only works for adding a missing sampling but also can eliminate the vibration of cutting due to noise or interference at the cutting threshold as Figure 7:

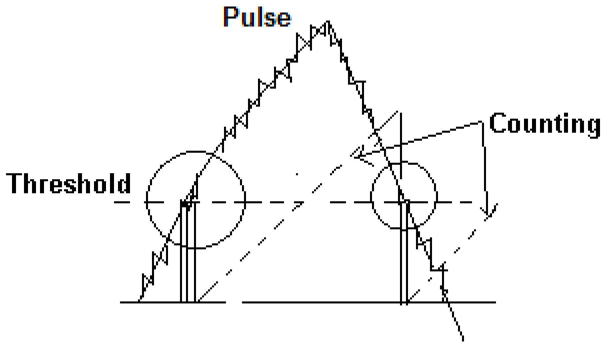


Fig. 7. The cutting threshold for the signal with noise

After amplification if the signal is smooth, the cutting threshold will give the clear rectangular pulses. If the signal is interfered, especially after shifted frequency up to 2.4 Ghz and down to the baseband of the receiver, around the cutting threshold there may have some narrow pulses. These narrow pulses can not be used directly as sampling pulses, it only uses for reset pins of the counter and the counter only starts to increase from the last narrow pulse of the rectangular slope. When the counter reaches to preset value (timing in the middle of the pulse), it will give only a sampling for rectangular pulse to avoid the vibration.

III. EXPERIMENT AND EVALUATION

The above design diagram is accomplished both on MATLAB and System Generator software. After converting into file.BIN, it is embedded in a FPGA chip (Virtex 4), then connected to a transmitter 2.4GHz frequency via DAC Card VHS (company Lyrtech). Figure 8 shows the complete diagram of the system.

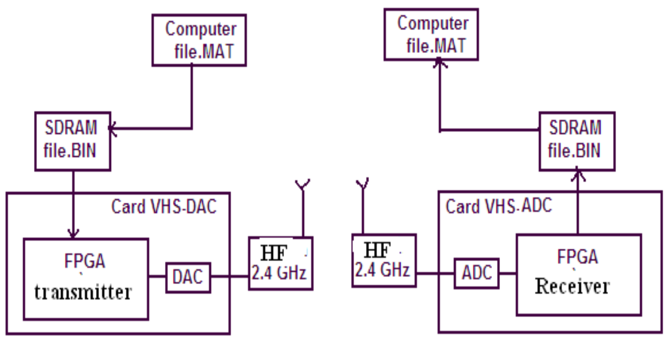


Fig. 8. The complete diagram of the system

a) The experimental data is 256×256 image (64Kbit):

Fig. 9. The transmitted image

Matlab environment used to convert an image from matrix to vector under *file.MAT* type. Then, *file.MAT* will be converted to *file.BIN* before downloaded into the SDRAM and FPGA chip to achieve high read-out speed respectively [4][5]. At the receiver, the process will be reversed.

The high frequency unit is the commercial transceivers with the low cost. These transceivers operate at the center frequency of 2.4GHz with FM modulation, bandwidth of 2MHz and input voltage is 0.5 –1V. Nevertheless, it is more expensive if the experiment is designed for the OFDM technique at high frequency unit using IQ modulation with high linearity.

Figure 10 is the received image, the obtained result in a 18dB-dynamic range of SNR is accurate.

Fig. 10. The received image

Data rate of the design diagram is calculated by: Primary Clock of VHS = 100MHz, the upsampling is 8 times (converted from pixel to bit) and 8 times for shaping filters, the output data rate will be: 100/(8×8) = 1.5Mb/s. This rate is prepared to match with the available bandwidth of the 2.4GHz frequency.

When the magnitude of input signal changes in the range of 18dB, the received image is always accurate. It means that the subtraction of the pixel matrix in transmitter and receiver absolutely equals to zero. This paper focuses on synchronous of the design diagram without feedback loops so it does not check the bit error rate (BER) under SNR when the incoming signal is too small.

b) Scalability of the method for high-speed data transfer using UWB pulses

The information in transmission process is the slope of rectangular pulse. Hence, if the slope of the rectangular pulses in Manchester code is replaced by differential narrow pulses (UWB), the diagram can give high data rate because this differential pulse may be designed for making narrow gap. For the capacities of Virtex 4, the proposed method can reach to 50Mb/s.

IV. CONCLUSION

In this paper, we proposed a simple diagram for data transmission using Manchester code. After evaluation, the proposed diagram works well even with wide dynamic input signal range of 18dB. Moreover, it is simple, notably without any feedback loops but still remains stable and can be extended for UWB modulation. For future work, we will carry out detail with the UWB pulse.

REFERENCES

[1] K. H. Mueller and M. S. Muller,"Timing Recovery in Digital Synchronous Data Receivers," *IEEE Transactions on Communications*, vol. 24, Issue 5,pp. 516-531, May 1976.

[2] F. M. Gardner, "A BPSK/QPSK Timing Error Detector for Sampled Receivers," *IEEE Transactions on Communications*, vol. 34, Issue 5, pp. 423-429, May 1986.

[3] Xilinx Core Generator System, http://www.xilinx.com/products/logicore/coregen/index.htm

[4] The MathworksInc, Simulink, Dynamic System Simulation for Matlab, Using Simulink, Natick, Massachusetts, USA, 1999.

[5] H. Fred and D. Chris, "On Structure and Implementation of Algorithms for Carrier and Symbol Synchronization in Software Defined Radios", *10th European Signal Processing Conference*, Tampere, Finland, September 2000.