A 300 GHz Single Varactor Doubler in 40 nm CMOS

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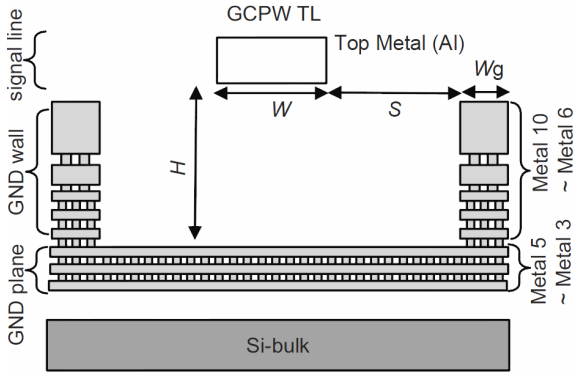
***Abstract*—This paper presents a 300 GHz single varactor doubler suitable for ultrahigh-speed wireless communications. The proposed varactor doubler realized in TSMC 40 nm CMOS can be integrated with other CMOS components to generate millimetter-wave signals at 300 GHz frequency band. At the pumping frequency of 150 GHz, input power of 10 dBm, the doubler results in an output power of -3.5 dBm at 300 GHz. The doubler consumes no DC power while it occupies a chip area of 0.27 mm^2 including probe pads.**

***Index Terms*—Doubler, Varactor, Frequency Multiplier, Millimeter-wave, 300 GHz, Ultrahigh-Speed**

I. Introduction

According to the current trend, frequency used for wireless communication will reach terahertz band in 2020. Unallocated frequency region beyond 275 GHz with vast bandwidth can be potentially utilized for ultrahigh-speed wireless communication. In particular, 300 GHz band is attractive since propagation decay in air around 300 GHz is relatively low. However, since studies on terahertz wireless communication including 300 GHz band are still in early stage when only a few transceivers operating above 275 GHz were reported. Since the maximum operating frequency or unity-power-gain frequency, f_{max}, of the n-type MOSFET even with advanced CMOS process is below 300 GHz, realization of 300 GHz RF front-end is challenging. One of common approaches is the use of frequency multipliers pumped by a high-power lower-frequency oscillator/amplifier. Active multipliers although promising, consume DC power and suffer from excessive resistive loss above process f_T/f_{max} leading to poor efficiency [1] [2]. Several frequency multipliers were reported using passive triplers [3]. However, the tripler generates not only the desired RF signal but also the higher-order spurious. As a result, the RF signal may be distorted by a higher-order spurious. On the other hand, since quadratic nonlinearity of a varactor is stronger than its cubic counterpart, a doubler can generate higher output power than a tripler does. In addition, the doubler can be realized without any idlers reducing circuit complexity.

In this paper, we are going to present the designs and measurement results of a 300 GHz single varactor doubler. When the doubler is employed, the 300 GHz output signal can be generated from the 150 GHz input one.



	50-Ω TL	71-Ω TL
W [μm] :	9.0	2.9
S [μm] :	7.2	7.6
Wg [μm] :	2.7	1.8
H [μm] :	7.0	7.0

Fig. 1. The cross-view of the GCPW-TLs.

II. Design of 300 GHz Single Varactor Doublers

A. Technology and Transmission Lines

The single 300 GHz varactor doubler is designed using TSMC 40 nm 1P10M CMOS GP process. Its back end consists of 10 copper layers and a top aluminum redistribution layer (RDL). The cross-view of grounded coplanar wave-guide transmission lines (GCPW-TLs) are depicted in Fig. 1. The GCPW-TL with the characteristic impedance of 50 Ω (the 50 Ω GCPW-TL) is used for connecting to the input and output pads of the 300 GHz doubler. Its signal line consists of the RDL layer with a width of 9 μm. Ground (GND) walls composed of the 6th to 10th metal layers with a width of 2.7 μm are placed on the both side of the signal line at the distance of 7.2 μm. The GCPW-TL with the characteristic impedance of 71 Ω (the 71 Ω GCPW-TL) is used for the shunt and series stubs of the doubler's matching networks and frequency reflectors. The width of the top-layer signal line is 2.9 μm, and the GND wall placed at a distance of 7.6 μm from the signal line has the width of 1.8 μm. The 3nd to 5th metal layers are meshed and stitched together with vias to form the GND plane. Electromagnetic (EM) simulation by ANSYS HFSS shows that the attenuation constant, α, of the 50 Ω and 71 Ω GCPW-TLs is 1.0–1.4 dB/mm and 1.2–1.6 dB/mm at 100–150 GHz, respectively.

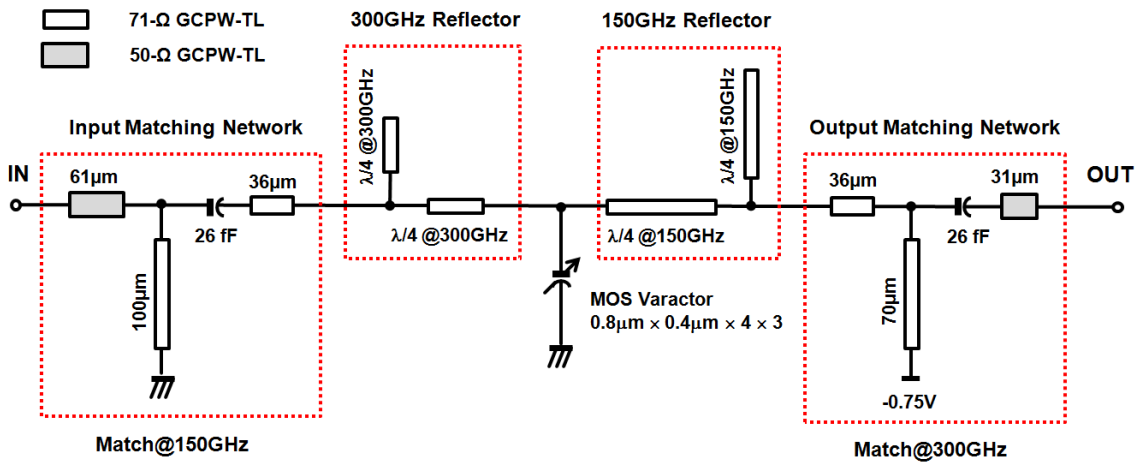


Fig. 2. The proposed single varactor doubler.

B. 300 GHz Single Varactor Doubler

As the name suggest, the 300 GHz varactor doubler exploits the quadratic nonlinearity of the varactors. It upconverts the signal at its input into RF signal at 300 GHz frequency band. The complete circuit of the proposed varactor doubler with all component values are given in Fig. 2. It includes a MOS varactor, two frequency reflectors, an input matching network and an output matching network. The varactor dimension, bias voltage and termination impedances are optimized using harmonic load-pull simulation to maximize the output power. All of the capacitors also act as coupling capacitors while the DC bias voltage is applied through the shunt stub of the output matching network. The far end of that shunt stub is terminated by a wideband decoupling power line with very low characteristic impedance (the 0 Ω TL). The second harmonic signal travelling back to the input port is reflected by the 300 GHz reflector. On the other hand, the fundamental frequency signal leaked through the varactor to the outpput port is reflected by the 150 GHz reflector. The lengths of the GCPW-TLs of the frequency reflectors are 150 μm and 300 μm which are equivalent to $\lambda/4$ (λ is the wave length) at 300 GHz and 150 GHz, respectively. The output is tuned to the second harmonic while other harmonics are further suppressed by the output matching network. The connection between the varactor, GCPW-TLs and MOM capacitors are made by the 8th to 10th metal layers. The compact design is realized by folding the GCPW-TLs and sharing the GND wall. The near-end and far-end crosstalk simulated by EM simulation are below -30 dB and -34 dB at 100 GHz and 250 GHz, respectively. It indicates that the cross-coupling between GCPW-TLs is negligible.

III. Measurement Results

In order to verify the performance of the single varactor doubler, a chip prototype was fabricated in TSMC 40 nm CMOS without any process modifications. The doubler weas measured by means of on-chip probing using a probe station. The RF probe pads were designed for ground-signal-ground (GSG) probes with 750 μm pitch. A Anritsu 37397D VNA, D-band and Y-band frequency extenders were used for measuring one-port S-parameters. Fig. 3 shows the die microphotograph of the varactor doubler. The doubler occupies an area of 0.6×0.45 mm^2 including probe pads while its core is only 0.05 mm^2. Fig. 4 plots the measured and simulated input return loss, S_{11}, of the single doubler from 130 GHz to 170 GHz. S_{11} remains below -10 dB for frequencies between 145 GHz and 163 GHz. Fig. 5 shows the measured and simulated output return loss, S_{22}, from 270 GHz to 330 GHz. S_{22} is less than -10 dB over the frequencies from 280 GHz to 310 GHz. As can be seen in these two figures, both S_{11} and S_{22} indicate wideband performances and the measured results show good agreements with the simulated ones.

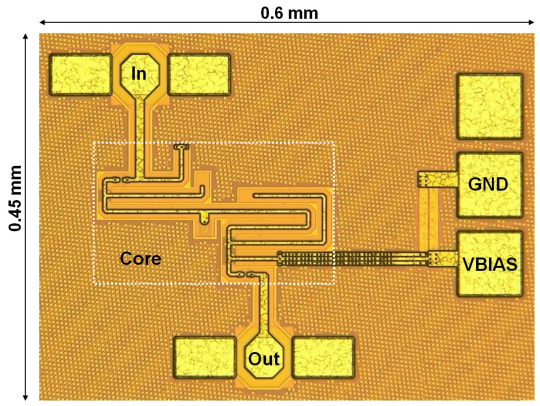


Fig. 3. The die microphtograph of the single varactor doubler.

Fig. 6 plots the output power versus the input power of the varactor doubler. A Keysight E8244A signal generator and a VivaTech VTXFA-06-12 signal module were used for generating input signal at 150 GHz while a VDI PM5-305V power sensor was used to measure the output power. At low input powers, the measured results show some discrepancies with the simulated ones due to the limitation of measurement equipments. The P_{out} of -3.5 dBm at 300 GHz is obtained with

TABLE I
COMPARISON WITH PREVIOUS PUBLISHED FREQUENCY MULTIPLIERS OPERATING AT SIMILAR FREQUENCY BAND

Parameter	EuMIC'09 [4]	ISSCC'11 [5]	JSSC'11 [1]	T-MTT'11 [2]	ISSCC'12 [6]	**This work**
Technology	50 nm GaAs	45 nm CMOS	65 nm CMOS	130 nm SiGe	65 nm CMOS	**40 nm CMOS**
Topology	Active doubler	Push-push oscillator	Active doubler	Active doubler	Harmonic oscillator	**Passive doubler**
Center Frequency (GHz)	300	291	244	325	290	**300**
Conversion Loss (dB)	7.4	N/A	11.4	4 (gain)	N/A	**13.5**
Output Power (dBm)	-6.4	-17	-6.6	-3	-1.2	**-3.5**
Die Area (mm^2)	0.38	0.16	0.02	0.51	0.36	**0.27**
Power Consumption (mW)	N/A	18.7	40	420	325	**0**

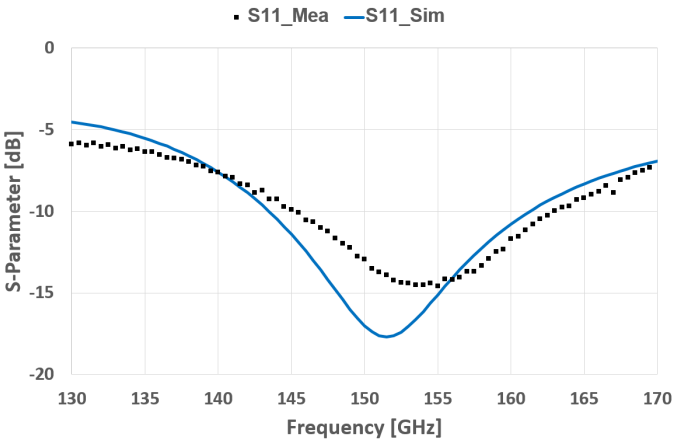


Fig. 4. The measured and simulated input return loss of the 300 GHz single varactor doubler.

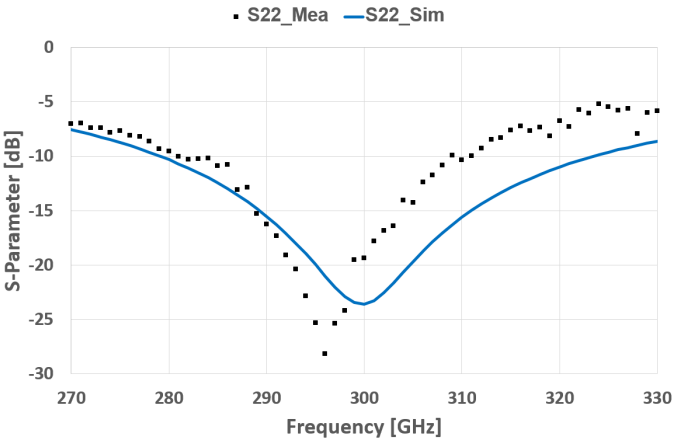


Fig. 5. The measured and simulated output return loss of the 300 GHz single varactor doubler.

the input power of 10 dBm resulting in conversion loss of 13.5 dB. Table I summarizes the performance of the proposed doubler and compares it to other published works operating in a similar frequency range.

IV. CONCLUSIONS

In this paper, we have presented the designs and measurement results of the 300 GHz single varactor doubler targeted for ultrahigh-speed wireless communications. The doubler was fabricated in TSMC 40 nm CMOS. Its core occupies a chip area of only 0.05 mm^2. Measurement results show that

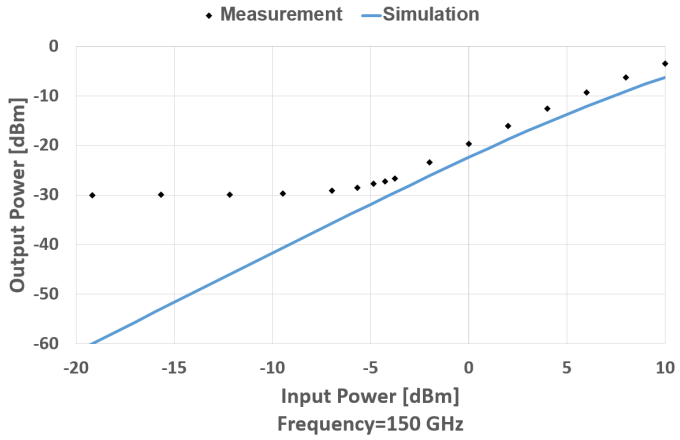


Fig. 6. The measured and simulated output power versus input power of the 300 GHz single varactor doubler.

the single varactor doubler archives the P_{out} of -3.5 dBm at 300 GHz while consuming no DC power. Compared to active frequency multipliers, varactor multipliers are capable of higher efficiency and higher output power.

ACKNOWLEDGEMENT

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REFERENCES

[1] O. Momeni and E. Afshari, "A broadband mm-wave and terahertz traveling-wave frequency multiplier on cmos," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2966–2976, December 2011.

[2] E. Ojefors, B. Heinemann, and U. R. Pfeiffer, "Active 220- and 325-ghz frequency multiplier chains in an sige hbt technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 5, pp. 1311–1318, May 2011.

[3] Z. Ahmad, I. Kim, and K. K. O, "0.39-0.45thz symmetric mos-varactor frequency tripler in 65-nm cmos," *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2015)*, pp. 275–278, May 2015.

[4] I. Kallfass, A. Tessmann, H. Massler, D. Lopez-Diaz, A. Leuther, M. Schlechtweg, and O. Ambacher, "A 300 ghz active frequency-doubler and integrated resistive mixer mmic," *European Microwave Integrated Circuits Conference (EuMIC 2009)*, pp. 200–203, September 2009.

[5] K. Sengupta and A. Hajimiri, "Distributed active radiation for thz signal generation," *2012 IEEE International Solid-State Circuits Conference (ISSCC 2011)*, pp. 288–289, February 2011.

[6] Y. M. Tousi, O. Momeni, and E. Afshari, "A 283-to-296ghz vco with 0.76mw peak output power in 65nm cmos," *2012 IEEE International Solid-State Circuits Conference (ISSCC 2012)*, pp. 258–259, February 2012.