Japanese Journal of Applied Physics **51** (2012) 09LA09 **REGULAR PAPER**
http://dx.doi.org/**10.1143/JJAP.51.09LA09**

Electric Properties and Interface Charge Trap Density of Ferroelectric Gate Thin Film Transistor Using $(Bi,La)_4Ti_3O_{12}/Pb(Zr,Ti)O_3$ Stacked Gate Insulator

Pham Van Thanh[1,4], Bui Nguyen Quoc Trinh[2,5*], Takaaki Miyasako[2], Phan Trong Tue[2,3], Eisuke Tokumitsu[2,3], and Tatsuya Shimoda[1,2,3]

[1]*School of Materials Science, Japan Advanced Institute of Science and Technology, Nomi, Ishikawa 923-1292, Japan*
[2]*ERATO, Shimoda Nano-Liquid Process Project, Japan Science and Technology Agency, Nomi, Ishikawa 923-1211, Japan*
[3]*Green Devices Research Center, Japan Advanced Institute of Science and Technology, Nomi, Ishikawa 923-1292, Japan*
[4]*Faculty of Physics, College of Science, Vietnam National University, Hanoi, Vietnam*
[5]*Faculty of Engineering Physics and Nanotechnology, College of Engineering and Technology, Vietnam National University, Hanoi, Vietnam*

Received May 25, 2012; accepted June 20, 2012; published online September 20, 2012

We successfully fabricated ferroelectric gate thin film transistors (FGTs) using solution-processed $(Bi,La)_4Ti_3O_{12}$ (BLT)/$Pb(Zr,Ti)O_3$ (PZT) stacked films and an indium–tin oxide (ITO) film as ferroelectric gate insulators and an oxide channel, respectively. The typical n-type channel transistors were obtained with the counterclockwise hysteresis loop due to the ferroelectric property of the BLT/PZT stacked gate insulators. These FGTs exhibited good device performance characteristics, such as a high ON/OFF ratio of 10^6, a large memory window of 1.7–3.1 V, and a large ON current of 0.5–2.5 mA. In order to investigate interface charge trapping for these devices, we applied the conductance method to MFS capacitors, i.e., Pt/ITO/BLT/PZT/Pt capacitors. As a result, the interface charge trap density (D_{it}) between the ITO and BLT/PZT stacked films was estimated to be in the range of 10^{-11}–10^{-12} eV^{-1} cm^{-2}. The small D_{it} value suggested that good interfaces were achieved.

1. Introduction

Recently, ferroelectric-gate field-effect transistors using ferroelectric materials as gate insulators have attracted much attention as a nonvolatile memory element with low power consumption, high speed, and high endurance owing to their natural ferroelectric properties, and there are various applications of these devices.[1,2] Si-based ferroelectric gate transistors have been studied most intensively.[3,4] However, Si-based ferroelectric gate transistors have the problem of interdiffusion of constituent elements between the ferroelectric layer and the Si substrate. To solve this problem, multistacked structures including a buffer layer, such as metal–ferroelectric–insulator–semiconductor (MFIS)[5] or metal–ferroelectric–metal–insulator–semiconductor (MFMIS)[6] structures, have been used to fabricate Si-based ferroelectric gate memory transistors. In the case of the MFIS structure, the problem of these transistors is charge mismatch between the ferroelectric layer and the insulator layer that leads to a small memory window in transfer characteristics even if a high operation voltage is applied.[7] In the case of the MFMIS structure, several reports have demonstrated good electrical properties,[3,4,6] such as a large memory window and a good retention time with a large MIS/MFM area ratio. However, it is complicated to fabricate; thus, it is not suitable for low-cost fabrication and high integration.

In order to solve the problems of the Si-based ferroelectric gate transistors, oxide-based ferroelectric gate thin film transistors (FGTs) could be one of the most promising candidates for a low-cost memory with high performance because of a very simple oxide–semiconductor/ferroelectric stacked structure. In addition, as the oxide–semiconductor layer can be deposited directly on the ferroelectric layer, these FGTs can utilize full ferroelectric polarization without charge mismatch because the polarization of the ferroelectric gate insulator can be directly applied to the oxide–semiconductor channel. The good properties of these typical FGTs have already been reported by Tokumitsu *et al.*,[7] Tanaka *et al.*,[8] Miyasako *et al.*[9] and Kato *et al.*[10] In order to reduce the processing costs, Miyasako *et al.* fabricated a total solution deposition-processed FGT using an indium–tin oxide (ITO)/$Pb(Zr,Ti)O_3$ (PZT) stacked structure with a large memory window and a high ON/OFF current ratio.[11] However, the existence of the 5-nm-thick interface layer between ITO and PZT resulted in a large interface charge trap density, leading to the inferior properties of this FGT. To obtain a better interface between the ITO channel and the gate insulator, we applied the BLT/PZT stacked structure, which was also processed by a solution method, as a gate insulator. To determine whether an interface between a semiconductor and an insulator layer is good, measuring the interface charge trap density (D_{it}) would be the best way. To calculate the D_{it} of a semiconductor/insulator structure, the conductance method using the admittance measurement of the metal–insulator–semiconductor (MIS) structure is a reliable technique.[12] Conventionally, SiO_2/Si is used to be the only MIS structure applied. Recently, however, this method has successfully been applied to investigate the D_{it} values of the polyfluorene-based MIS,[13] Ge-based MIS,[14] and metal–ferroelectric–semiconductor structures.[15] Therefore, it is suitable to use this method to investigate the D_{it} of the ITO/BLT/PZT structure, i.e., the metal–ferroelectric–semiconductor structure.

In this study, we first tried to fabricate an FGT that used a BLT/PZT stacked gate insulator and demonstrated that it had a high ON/OFF ratio and a large memory window. Then, by applying the conductance method using the admittance measurements of the Pt/ITO/BLT/PZT/Pt (MFS) capacitors, the interface charge trap density (D_{it}) between the ITO and BLT/PZT stacked ferroelectric gate insulators was found to be as small as that in the 10^{11}–10^{12} eV^{-1} cm^{-2} range. This fact confirmed that the good interfaces were realized.

2. Experimental Procedure

BLT/PZT hybrid films were prepared on Pt(111)/Ti/SiO_2/Si substrates by the sol–gel technique. First, the raw solution of $Pb_{1.2}(Zr_{0.4}Ti_{0.6})O_3$ (PZT) was spin-coated at a speed

*E-mail address: trinhbnq@vnu.edu.vn

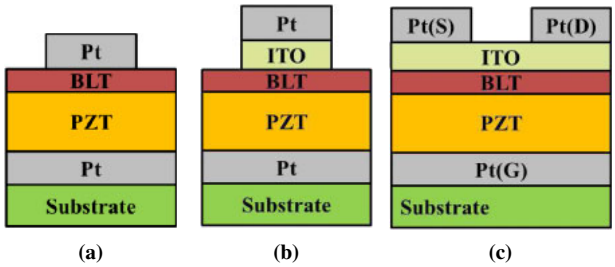

Fig. 1. (Color online) Schematic illustrations of (a) MFM, (b) MFS capacitors, and (c) FGT using BLT/PZT stacked structure as gate insulator.

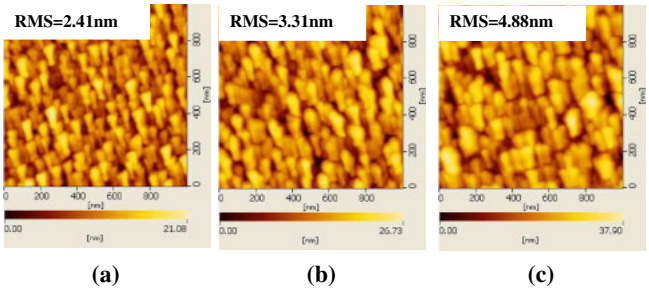

Fig. 2. (Color online) AFM images of (a) 20-, (b) 40-, and (c) 60-nm-thick BLT films on PZT/Pt/Ti/SiO_2/Si.

of 2500 rpm for 25 s and dried at 240 °C for 5 min. This process was repeated several times to obtain a 170-nm-thick PZT film, and then the film was crystallized at 600 °C for 20 min in air by rapid thermal annealing (RTA). Excess lead was added to compensate for evaporation loss and to assist the crystallization. Secondly, the raw solution of $Bi_{3.35}La_{0.75}Ti_3O_{12}$ (BLT) was spin-coated at a speed of 2000 rpm for 30 s and dried at 250 °C, the thickness of the BLT film was changed from 20 to 60 nm, and then the BLT film was crystallized at 675 °C for 10 min in O_2 by RTA. Then, the ITO layer with a thickness of 25 nm was deposited by spin coating the carboxylate-based precursor solution (5 wt % SnO_2-doped) on the BLT/PZT hybrid film and consolidated at 350 °C in air for 10 min. Subsequently, the Pt source and drain electrodes were sputtered at room temperature and patterned by a lift-off process. In the next step of fabrication, the ITO channel was isolated by photolithography and dry etching. Finally, the ITO channel was annealed at 450 °C in air for 40 min by RTA. The channel length (L_{DS}) and the channel width (W) were 15 and 60 μm, respectively. The schematic illustrations of Pt/BLT/PZT/Pt (MFM) and Pt/ITO/BLT/PZT/Pt (MFS) capacitors with top electrodes of 1.12×10^{-4} cm^2 area and an FGT are shown in Figs. 1(a)–1(c).

The morphology of these samples was investigated by atomic force microscopy (AFM) analyses using the SII-NT SPA400 system. The polarization–electric field (P–E) curves were measured using the Sawyer–Tower circuit. The capacitance–voltage (C–V) measurements were performed using Wayne Kerr precision component analyzer 6440B with an AC signal of 50 mV amplitude. The impedance characteristics were determined using the Solartron 1296 dielectric interface and 1260 impedance analyzer in a frequency range of 5 Hz–100 kHz at room temperature with an AC signal of 50 mV amplitude. These measurements were carried out by applying voltage to the bottom Pt electrode with the top Pt electrode grounded. The transfer characteristics (I_D–V_G) and the output characteristics (I_D–V_D) were measured using a semiconductor parametric analyzer (Agilent 4155C).

3. Results and Discussion

The AFM analysis was carried out to investigate the morphology of the fabricated BLT/PZT stacked films. The obtained AFM images are shown in Figs. 2(a)–2(c). It is seen that all BLT films show good uniformity without cracks or fissures. The root-mean-square (RMS) surface roughness values were 2.41, 3.31, and 4.88 nm, which correspond to the 20, 40, and 60 nm BLT layer thicknesses, respectively; these RMS surface roughness values are smaller than those of the pure BLT films.[16–18]

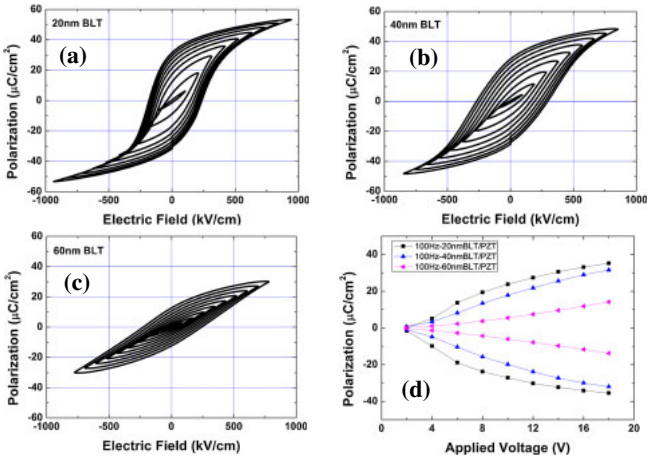

Fig. 3. (Color online) P–E loops of MFM capacitors with (a) 20, (b) 40, and (c) 60 nm BLT layer thicknesses. The measurement frequency was 100 Hz. (d) Values of P_r vs applied voltage of MFM capacitors.

Figures 3(a)–3(c) show the P–E loops of the Pt/BLT/PZT/Pt capacitors. These P–E loops have good square shapes. In addition, the values of remanent polarization (P_r) vs applied voltages of these capacitors are shown in Fig. 3(d). The values of P_r measured at 10 V were 23.9, 17.8, and 6.5 μC/cm^2 for the 20, 40, and 60 nm BLT layer thicknesses, respectively. It was observed that P_r decreased as the thickness of the BLT layer increased. The dielectric constant of the BLT film was about 138–350,[19,20] which is much smaller than that of the PZT film,[21] which lies between 700 and 1300. Therefore, the applied voltage can be reduced markedly in the BLT layer of the BLT/PZT structure, in which the BLT layer is serially connected with the PZT layer. This means that a large polarization of the BLT/PZT capacitor is only achieved when the BLT layer is thin enough.[22] Simultaneously, the C–V characteristics of these samples were also investigated and are shown in Fig. 4. The butterfly shape of these C–V characteristics was obtained owing to the natural ferroelectric property of the BLT/PZT structures. The capacitances also decreased as the thickness of the BLT layer increased because of the serial connection of the BLT layer with the PZT layer.

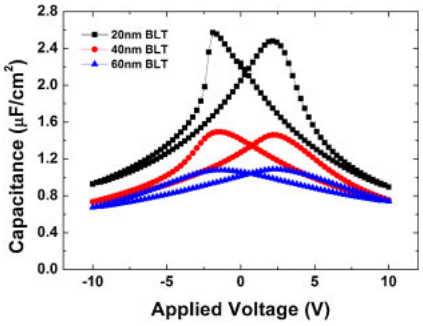

Fig. 4. (Color online) *C*–*V* characteristics of Pt/BLT/PZT/Pt capacitors.

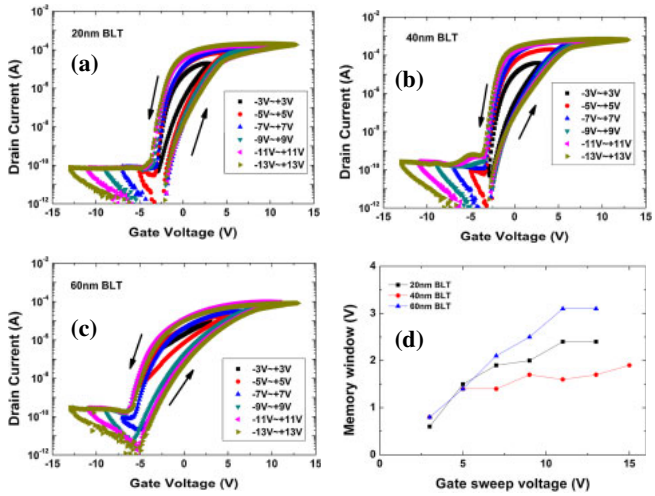

Fig. 5. (Color online) I_D–V_G characteristics of FGTs with (a) 20, (b) 40, and (c) 60 nm BLT layer thicknesses. (d) Memory window vs gate sweep voltage.

Figures 5(a)–5(c) show the I_D–V_G characteristics of these fabricated FGTs when the gate voltage sweep changed from the narrow range (from −3 to 3 V) to the wide one (from −13 to 13 V) with a constant drain voltage (V_D) of 1.5 V. The counterclockwise hysteresis loops were obtained for all samples owing to the natural ferroelectric properties of the BLT/PZT gate insulators. This result confirmed the nonvolatile memory function of these FGTs. The high ON/OFF ratios of $\sim 10^6$ and the large memory windows of 1.7–3.1 V were obtained [Fig. 5(d)]. Notably, the OFF currents of these FGTs were as small as 10^{-10} A despite the large charge concentration of the ITO channels of around 10^{19} cm^{-3}.[11] These OFF currents are significantly smaller by 3 orders of magnitude than that of the FGT using the ITO/BLT structure.[7] This means that the ITO channels were completely depleted by the huge polarization charges of the BLT/PZT stacked gate insulators. The S-swings of these FGT were also obtained and are shown in Table I.

Simultaneously, the I_D–V_D characteristics of these FGTs were determined with the sweep of V_D from 0 to 10 V by changing V_G from 0 to 8 V [Figs. 6(a)–6(c)]. It was observed that a typical n-channel transistor operation was obtained with a large ON current for all fabricated FGTs. At $V_D = 10$ V and $V_G = 8$ V, the ON currents were estimated to be in the range of 0.5–2.5 mA, which is close to those

Table I. Device characteristics of fabricated FGTs using ITO/BLT/PZT structures when the thickness of BLT layer was varied to 20 nm (FGT1), 40 nm (FGT2), and 60 nm (FGT3).

Sample	Field-effect mobility (cm^2 V^{-1} s^{-1})	Threshold voltage (V)	S-swing (mV/dec)	ON/OFF ratio ($V_D = 1.5$ V, $V_G = 9$ V)	Memory window (V)
FGT1	6.5	1.5	600	2.2×10^6	2
FGT2	6.3	1.7	630	2×10^6	1.7
FGT3	3.9	1.7	1320	2.8×10^5	2.5

of the other TFTs using the oxide semiconductor as the channel.[9,23] In addition, the field-effect mobility μ_{FE} of the ITO channel was estimated in the saturation region of the drain current, which is given by[7]

$$I_{DS} = \mu_{EF} \frac{W}{2L} \frac{P(V_G)}{V_G} (V_G - V_T)^2, \quad (1)$$

where I_{DS} is the drain current in the saturation region of the output characteristics, V_T is the threshold voltage obtained by a linear fit of the square root of the drain current vs gate voltage of the I_D–V_G characteristics[24] (Table I), and $P(V_G)$ is the ferroelectric polarization as a function of the gate voltage (V_G), which can be obtained from the *P*–*E* loop of the BLT/PZT capacitor. With $V_G = 8$ V, $P(V_G)$ was approximately determined to be 36, 27, and 15 μC/cm^2; therefore, μ_{FE} was estimated to be 6.5, 6.3, and 3.9 cm^2 V^{-1} s^{-1}, which correspond to the 20, 40, and 60 nm BLT layer thicknesses, respectively. The reason for the degradation of the μ_{FE} of these FGTs with increasing BLT layer thickness could be the rough surface of the BLT/PZT stacked insulator films. It was observed that the RMS surface roughness significantly increased from 2.41 to 4.88 nm with increasing thickness of the BLT layer from 20 to 60 nm (Fig. 2), which leads to the enhancement of electron scattering at the semiconductor/insulator interface of the FGTs. The effect of dielectric roughness on the mobility of thin film FETs has been discussed elsewhere.[25–27] These μ_{FE} values are comparable to those of the other TFTs using oxide semiconductors, such as sputter ITO,[7,9] ZnO,[23,28] and IGZO.[29,30] Although the field-effect mobility of the ITO channel is small, the large ON currents of mA order were obtained [Figs. 6(a)–6(c)] because the huge polarization of the ferroelectric gate insulator can be applied directly to the channel. Some important parameters of these FGTs are summarized and listed in Table I with a gate voltage sweep of ±9 V.

To further confirm the depletion and accumulation characteristics of the ITO layers, the *C*–*V* characteristics of the MFS capacitors, which are illustrated in Fig. 1(b), were investigated. The measured curves plotted as square-line curves are shown in Figs. 7(a)–7(c) with those of the MFM capacitors as references (circle-line curves) when the thickness of the BLT layer changed. These *C*–*V* characteristics exhibited a large difference between the negative and positive applied voltages for all samples. When the positive voltage was applied, the capacitance of the MFS capacitors (C_{on}) was approximate to that of the MFM capacitors, indicating that the electrons accumulated in the ITO layer; whereas when the negative voltage was applied, the capacitance of the MFS capacitors (C_{off}) was much smaller

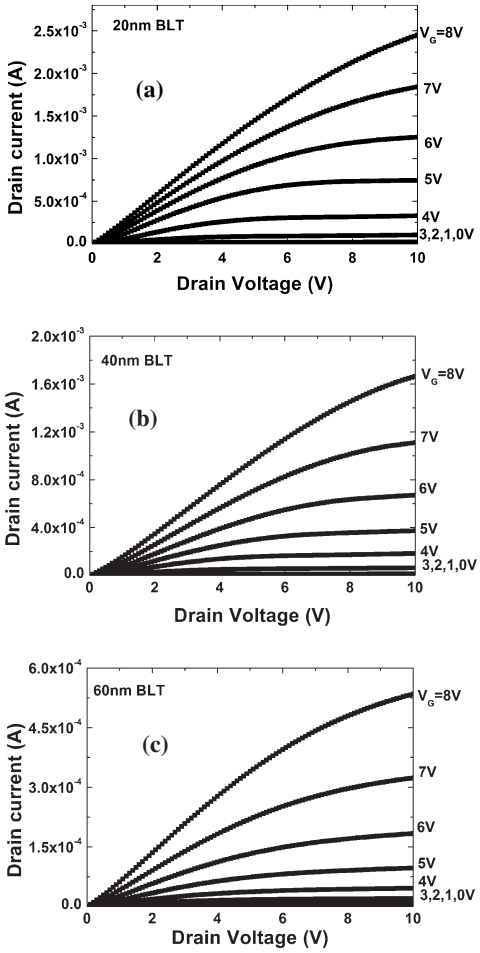

Fig. 6. I_D–V_D characteristics of the FGTs with (a) 20, (b) 40, and (c) 60 nm BLT layer thicknesses.

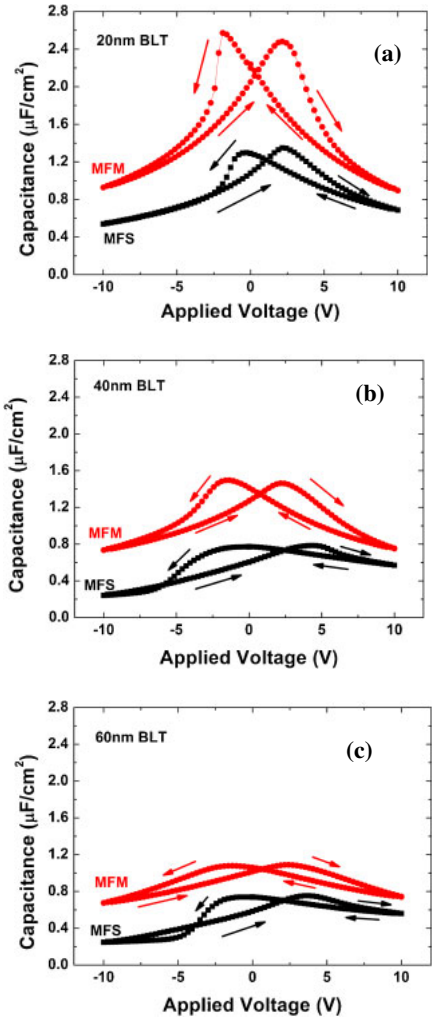

Fig. 7. (Color online) C–V characteristics of MFSs (square-line) and MFMs (circle-line) with (a) 20, (b) 40, and (c) 60 nm BLT layer thicknesses of the BLT/PZT stacked films.

than that of the MFM capacitors as a result of the depletion of the ITO layer.[10,31] Furthermore, the values of C_{off} are always smaller than those of C_{on} for all MFS capacitors. This difference between C_{on} and C_{off} indicated that the conductivity of ITO layers was completely controlled by the BLT/PZT stacked gate insulators. Such a difference is the origin of the ON/OFF operation of these FGTs.[32]

Next, the impedance characteristics of these MFS capacitors were measured, and their admittance characteristics were also obtained. As the MFS capacitors can be considered MIS capacitors when they are depleted, it is expected that the interface charge trap density (D_{it}) values of semiconductor (ITO)/ferroelectric insulator (BLT/PZT) contacts could be estimated in these MFS capacitors by the conductance method using the admittance characteristics. The parallel equivalent circuit of the MFS capacitors is shown in Fig. 8(a),[12] where C_{ox} is the capacitance of the ferroelectric-insulator layer, i.e., the BLT/PZT stacked layer, C_p and G_p are the equivalent parallel capacitance and equivalent parallel conductance, respectively, and R_s is the serial resistance. The equivalent parallel conductance G_p of the semiconductor portion of the MFS capacitors in the depleted region is given by[12]

$$\frac{G_p(\omega)}{\omega} = \frac{C_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2], \quad (2)$$

where C_{it}, τ_{it}, and ω are the interface trap capacitance, the interface trap response time, and the angular frequency, respectively. The peak of G_p/ω is equal to $0.4C_{it} = 0.4qD_{it}$ when $\omega\tau_{it} = 1.98$. However, G_p is not equal to the measured parallel conductance G_m of the measured admittance, $Y_m = G_m + j\omega C_m$, with C_m being the measured capacitance. G_p must be corrected from Y_m by using the parallel equivalent circuit of the MFS capacitors. Therefore, G_p/ω is calculated by

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_c}{G_c^2 + \omega^2 (C_{ox} - C_c)^2}, \quad (3)$$

where $C_c = (G_m^2 + \omega^2 C_m^2)C_m/(a^2 + \omega^2 C_m^2)$, $G_c = (G_m^2 + \omega^2 C_m^2)a/(a^2 + \omega^2 C_m^2)$, and $a = G_m - (G_m^2 + \omega^2 C_m^2)R_s$, with R_s being calculated from the measured admittance upon the accumulation of the MFS capacitors. Notably, the capacitance C_{ox} values of the BLT/PZT stacked films that show a butterfly-shaped curve depend on the applied voltages shown as the circle-line curves in Figs. 7(a)–7(c). In the depleted region of the MFS capacitors, however, the ITO layer is depleted; thus, it is difficult to determine the exact values of C_{ox}. To solve this problem, D_{it} should be calculated at the applied voltage of 0 V in the depleted region when the

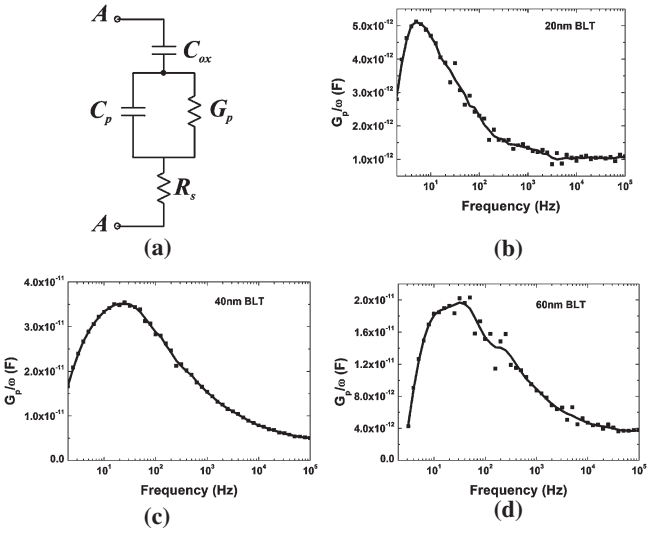

Fig. 8. (a) Equivalent circuit of MFSs. Values of G_p/ω vs frequency for (b) 20, (c) 40, and (d) 60 nm BLT layer thicknesses of MFS capacitors.

applied voltage is swept from −10 to 10 V. Consequently, the values of G_p/ω vs ω were calculated and are shown in Figs. 8(b)–8(d), where the peaks of G_p/ω are clearly seen. In these calculations, the values of C_{ox} were obtained from the impedance measurements of the MFM capacitors at the applied voltage of 0 V. From the peaks of G_p/ω, D_{it} was extracted to be 7.1×10^{11}, 4.8×10^{12}, and $2.7 \times 10^{12}\,eV^{-1}\,cm^{-2}$, which correspond to the 20, 40, and 60 nm BLT film thicknesses, respectively. These D_{it} values are comparable to those of MFIS[33] and MFMIS.[4] Notably, the D_{it} value of the MFS capacitor corresponding to that of the 60-nm-BLT/PZT stacked insulator is the largest, which seems to be one of the reasons for the smallest memory window of the FGT using this stacked film as the gate insulator. Because of the small D_{it} values, it is believed that the good interfaces between the ITO channel and the BLT/PZT stacked gate insulators were obtained. These results are in good agreement with the well-formed interface between the ITO channel and the BLT/PZT stacked gate insulator reported by Trinh *et al.*[34]

4. Conclusions

In this study, FGTs using solution-processed BLT/PZT stacked gate insulators and a sol–gel ITO channel were successfully fabricated and characterized. The high ON/OFF ratios of ~10^6 and the large memory windows of 1.7–3.1 V were obtained. The field-effect mobility of the channel was determined to be 6.5, 6.3, and 3.9 $cm^2\,V^{-1}\,s^{-1}$ as the thickness of the BLT layer was varied to 20, 40, and 60 nm, respectively. Furthermore, the *C*–*V* characteristics of the MFS capacitors reconfirmed the accumulation and depletion phenomena of the ITO layer of MFSs. In particular, by the conductance method, the charge trap density between the ITO layers and the BLT/PZT stacked gate insulators was determined to be as small as 10^{11}–$10^{12}\,eV^{-1}\,cm^{-2}$. This small charge trap density was found to result in the good properties of the FGT. Consequently, the FGT constructed by the combination of the ITO channel and the BLT/PZT stacked gate insulator would be a good candidate for the nonvolatile ferroelectric memory applications in the future.

Acknowledgment

This work was partially supported by the Japan Science and Technology Agency-ERATO-Shimoda Nano Liquid Project. P. V. Thanh gratefully acknowledges financial support by 322 Scholarships (doctoral course) of the Vietnamese Government.

1) J. F. Scott and C. A. Paz de Araujo: Science **246** (1989) 1400.
2) C. A. P. de Araujo, J. D. Cuchiaro, L. D. McMillan, M. C. Scott, and J. F. Scott: Nature **374** (1995) 627.
3) E. Tokumitsu, G. Fujii, and H. Ishiwara: Appl. Phys. Lett. **75** (1999) 575.
4) E. Tokumitsu, G. Fujii, and H. Ishiwara: Jpn. J. Appl. Phys. **39** (2000) 2125.
5) K. Aizawa, B.-E. Park, Y. Kawashima, K. Takahashi, and H. Ishiwara: Appl. Phys. Lett. **85** (2004) 3199.
6) E. Tokumitsu, K. Okamoto, and H. Ishiwara: Jpn. J. Appl. Phys. **40** (2001) 2917.
7) E. Tokumitsu, M. Senoo, and T. Miyasako: Microelectron. Eng. **80** (2005) 305.
8) H. Tanaka, Y. Kaneko, and Y. Kato: Jpn. J. Appl. Phys. **47** (2008) 7527.
9) T. Miyasako, M. Senoo, and E. Tokumitsu: Appl. Phys. Lett. **86** (2005) 162902.
10) Y. Kato, Y. Kaneko, H. Tanaka, and Y. Shimada: Jpn. J. Appl. Phys. **47** (2008) 2719.
11) T. Miyasako, B. N. Q. Trinh, M. Onoue, T. Kaneda, P. T. Tue, E. Tokumitsu, and T. Shimoda: Jpn. J. Appl. Phys. **50** (2011) 04DD09.
12) E. H. Nicollian and J. R. Brews: *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 1982) Chap. 5.
13) M. Yun, R. Ravindran, M. Hossain, S. Gangopadhyay, U. Scherf, T. Bünnagel, F. Galbrecht, M. Arif, and S. Guha: Appl. Phys. Lett. **89** (2006) 013506.
14) N. Taoka, W. Mizubayashi, Y. Morita, S. Migita, H. Ota, and S. Takagi: J. Appl. Phys. **109** (2011) 084508.
15) M. Alexe: Appl. Phys. Lett. **72** (1998) 2283.
16) S. Lin, X. Dingquan, Y. Ping, Z. Jianguo, G. Daojiang, Y. Guanglong, and Z. Wen: Mater. Trans. **44** (2003) 1324.
17) E. Tokumitsu, M. Senoo, S. Etsu, and T. Fujimura: Materials and Processes for Nonvolatile Memories II Symp., 2007, p. 237.
18) A. Z. Simões, C. S. Riccardi, L. S. Cavalcante, A. H. M. Gonzalez, E. Longo, and J. A. Varela: Mater. Res. Bull. **43** (2008) 158.
19) B. S. K. B. H. Park, S. D. Bu, T. W. Noh, J. Lee, and W. Jo: Nature **401** (1999) 682.
20) S.-T. Zhang, Z. Chen, C. Zhang, and G.-L. Yuan: Appl. Surf. Sci. **256** (2010) 2468.
21) J. Pérez de la Cruz, E. Joanni, P. M. Vilarinho, and A. L. Kholkin: J. Appl. Phys. **108** (2010) 114106.
22) B. T. Liu, X. Zhang, W. T. Zhang, Z. Yan, C. S. Cheng, F. Li, L. Li, and Q. X. Zhao: Mater. Lett. **61** (2007) 3045.
23) J. Siddiqui, E. Cagin, D. Chen, and J. D. Phillips: Appl. Phys. Lett. **88** (2006) 212903.
24) J. S. Lee, S. Chang, S.-M. Koo, and S. Y. Lee: IEEE Electron Device Lett. **31** (2010) 225.
25) A. B. Y. Chan, C. T. Nguyen, P. K. Ko, S. T. H. Chan, and S. S. Wong: IEEE Trans. Electron Devices **44** (1997) 455.
26) K. Okamura, N. Mechau, D. Nikolova, and H. Hahn: Appl. Phys. Lett. **93** (2008) 083105.
27) S. Steudel, S. De Vusser, S. De Jonge, D. Janssen, S. Verlaak, J. Genoe, and P. Heremans: Appl. Phys. Lett. **85** (2004) 4400.
28) T. Fukushima, T. Yoshimura, K. Masuko, K. Maeda, A. Ashida, and N. Fujimura: Jpn. J. Appl. Phys. **47** (2008) 8874.
29) G. H. Kim, B. Du Ahn, H. S. Shin, W. H. Jeong, H. J. Kim, and H. J. Kim: Appl. Phys. Lett. **94** (2009) 233501.
30) G.-G. Lee, Y. Fujisaki, H. Ishiwara, and E. Tokumitsu: Appl. Phys. Express **4** (2011) 091103.
31) S. Mathews, R. Ramesh, T. Venkatesan, and J. Benedetto: Science **276** (1997) 238.
32) T. Fukushima, T. Yoshimura, K. Masuko, K. Maeda, A. Ashida, and N. Fujimura: Thin Solid Films **518** (2010) 3026.
33) C.-Y. Chang, T. P.-C. Juan, and J. Y.-M. Lee: Appl. Phys. Lett. **88** (2006) 072917.
34) B. N. Q. Trinh, T. Miyasako, T. Kaneda, P. T. Tue, P. V. Thanh, E. Tokumitsu, and T. Shimoda: presented at Int. Symp. Integrated Functionalities 2011 (ISIF2011).