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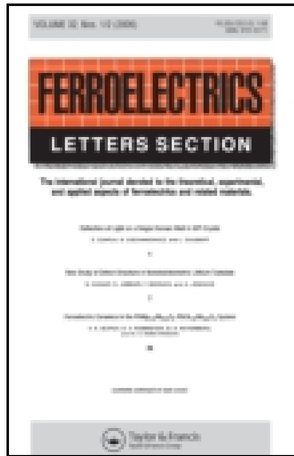

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Interface Charge Trap Density of Solution Processed Ferroelectric Gate Thin Film Transistor Using ITO/PZT/Pt Structure

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Interface Charge Trap Density of Solution Processed Ferroelectric Gate Thin Film Transistor Using ITO/PZT/Pt Structure

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The conductance method was applied to investigate the interface charge trap density (D_{it}) of solution processed ferroelectric gate thin film transistor (FGT) using indium-tin oxide (ITO)/ $Pb(Zr,Ti)O_3$ (PZT)/Pt structure. As a result, a large value of D_{it} of MFS capacitor, i.e., Pt/PZT/ITO, was estimated to be 1.2×10^{14} eV^{-1} cm^{-2}. This large D_{it} means that an interface between the ITO layer and the PZT layer is imperfect and it is one of the main reasons for the poor memory property of this FGT. By using transmission electron microscopy (TEM), this imperfect interface was clearly observed. Thus, it is concluded that improvement of this interface is critical for better memory performance.

Keywords Ferroelectric; metal-ferroelectric-semiconductor; indium-tin oxide (ITO); $Pb(Zr,Ti)O_3$(PZT); ferroelectric gate thin film transistor (FGT); *C-V* measurement; interface charge trap density (D_{it}); conductance method

1. Introduction

Recently, ferroelectric-gate field-effect transistors using ferroelectric materials as gate insulators have attracted much attention as a nonvolatile memory element with low power consumption, high speed and high endurance due to their natural ferroelectric properties,

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and there are various applications such as wireless IC cards and tools for mobile communication [1, 2]. Many studies of these devices have been conducted since the 1960s [3, 4]. Among these studies, Si-base ferroelectric gate transistors have been studied most intensively [5, 6]. However, Si-base ferroelectric gate transistors have the problem of interdiffusion of constituent elements between the ferroelectric layer and the Si substrate because high crystallization temperature is needed to deposit ferroelectric films leading to formation of a transition layer at the interface between the Si-substrate and the ferroelectric layer, therefore the interface charge trap density is increased very much when the crystallization temperature of ferroelectric films is increased [7]. It is well known that the interfaces between semiconductor channels and gate insulators of field effect transistors influent much on their electric properties [8–10]; thus, this transition layer leads to poor electric properties of this transistor. To solve this problem, multi-stacked structures including a buffer layer such as a metal-ferroelectric-insulator-semiconductor (MFIS) [11, 12] or a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) [13] have been used to fabricate Si-base ferroelectric gate memory transistors. In the case of the MFIS structure, C. Y. Chang *et al.* reported the small value of $3 \times 10^{11}eV^{-1}$ cm^{-2} of interface charge trap density between Si-semiconductor and Dy_2O_3 insulator of MFIS structure estimated by the conductance method [12]. However, a problem of these transistors is charge mismatch between the ferroelectric layer and the insulator layer. Therefore, partial polarization of a polarization-electric field (P-E) loop is only used in MFIS-FET structure [14]. That leads to a small memory window in transfer characteristics even if high operation voltage is applied. In the case of the MFMIS structure, several reports have demonstrated good electrical properties [5, 6, 13] such as large memory window and good retention time with the large MIS/MFM area ratio; especially, the small interface charge trap density of $1–2 \times 10^{12}$ eV^{-1} cm^{-2} calculated by C-V measurement was believed to be one of the major reasons for the improved electric properties of the MFMIS-FET [6]. However, its structure is complicated to fabricate, so it is not suitable for low-cost fabrication and high integration.

Therefore, oxide-based ferroelectric gate thin film transistor (FGT) could be one of the most promising candidates for a low cost memory with high performance, because of very simple oxide-semiconductor/ferroelectric stacked structure. In addition, as the oxide-semiconductor layer can be deposited directly on the ferroelectric layer, these FGTs can utilize full ferroelectric polarization without charge-mismatch because the polarization of the ferroelectric gate insulator can be directly applied to the oxide-semiconductor channel. Consequently, this type of FGTs could have large memory window with low operation voltage and improve retention properties. The good properties of these typical FGTs have been already reported by Tokumitsu *et al.* [14], Tanaka *et al.* [15], Miyasako *et al.* [16] and Kato *et al.* [17]. Furthermore, in order to reduce the processing costs, Miyasako *et al.* reported the total solution deposition processed-FGT using ITO/PZT stacked structure with a large memory window and a high ON/OFF current ratio [18]. The effect of the oxide-semiconductor/ferroelectric interface on the electric properties of these FGTs was also considered. Kato *et al.*[17] and Kaneko *et al.* [19] reported the very good interface between the ZnO layer and the PZT one deposited by PLD method, which was observed by the HR-TEM. This perfect interface leads to the good electric properties of these FGTs such as the large on/off ratios of 10^5, the good data retention properties: it is believed that the amount of space charge at the ZnO/PZT interface is markedly low. Whereas, Miyasako *et al.* reported the existence of the imperfect 4-nm-thick interface between the ITO channel and the PZT layer of the FGT fabricated by total solution process, which could result in the large interface charge trap and it was supposed to be a main reason for the poor retention property [18]. However, the absolute value of the interface charge trap density (D_{it}) between the oxide-semiconductor and the ferroelectric insulator has not yet reported

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before although this interface charge trap density (D_{it}) would be the best way to confirm whether a semiconductor/insulator interface is good or not. In order to determine the D_{it} between a semiconductor and an insulator, the conductance method extracted from the admittance measurement of the metal-insulator-semiconductor (MIS) structure is a reliable method [20], in which SiO_2/Si was used as a standard MIS structure. This method is useful not only for the Si-based MIS structure but also for the others, such as polyfluorene-based MIS [21] and Ge-base MIS [9]. In addition, by using the conductance method, the D_{it} of the metal-ferroelectric-semiconductor structure was also investigated [22]. Therefore, it is expected that this method could be used to calculate the D_{it} of ITO/PZT structure, i.e., metal-ferroelectric-semiconductor structure.

In this study, a good FGT was successfully fabricated using solution processed-PZT and sol-gel ITO as ferroelectric gate insulator and n-type channel, respectively. Electric properties of this FGT were investigated. The measured capacitance-voltage (C-V) characteristic of Pt/ITO/PZT/Pt (MFS) capacitor exhibited that depletion and accumulation of the ITO layer were wholly controlled by the huge polarization charge of the PZT-gate insulator. In particular the interface charge trap density (D_{it}) between ITO and PZT was estimated by using the conductance method.

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2. Experimental Methods

170-nm-PZT thin film was prepared on a Pt(111)/Ti/SiO_2/Si substrate by the sol-gel technique. Raw solution of $Pb_{1.2}(Zr_{0.4}Ti_{0.6})O_3$ was spin coated at a speed of 2500 rpm for 25 s, then dried at 240°C for 5 min, this process was repeated several times to obtain 170-nm-thick of PZT film, and then this sample was crystallized at 600°C for 20 min in ambient air by rapid thermal annealing (RTA) system. The excess of the lead was added to compensate for evaporation loss and to assist the crystallization. Next, the ITO layer with a thickness of 25 nm was deposited by spin-coating using carboxylate-based precursor solution (5 wt% SnO_2-doped) on the PZT layer and consolidated at 350°C in air for 10 min. After that, Pt source and drain electrodes were sputtered at room temperature and patterned by a lift-off process. In the next step of fabrication, the ITO channel was patterned by photolithography and dry-etching. Finally, the ITO channel was annealed at 450°C in air for 60 min by RTA. The channel length (L_{DS}) and channel width (W) were 15 and 60 μm, respectively. Schematic illustrations of Pt/PZT/Pt (MFM), Pt/ITO/PZT/Pt (MFS) capacitors with 1.12×10^{-4} cm^2 area of the top electrodes and a FGT are shown in Fig. 1(a)–1(c).

The crystalline structure of the PZT thin film was identified by X-ray diffraction (M18XHF-SRA) using Cu Kα radiation. The cross sectional image of an ITO/PZT/Pt structure was observed by the transmission electron microscope (TEM). The

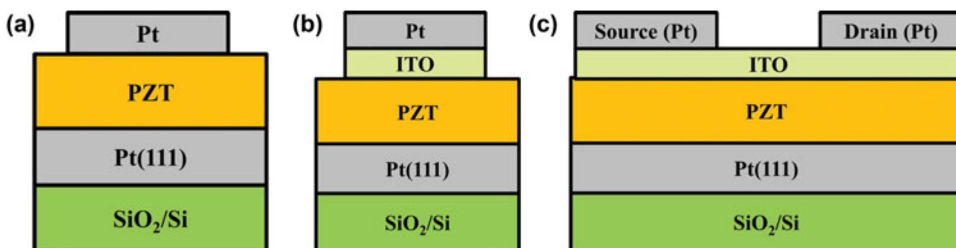

Figure 1. Schematic illustrations of (a) MFM, (b) MFS capacitors and (c) ferroelectric gate thin film transistor. (Figure available in color online.)

polarization-electric field (P-E) curves were measured using the Sawyer-Tower circuit. The capacitance-voltage (C-V) measurements were performed using Wayne Kerr precision component analyzer 6440B with 50 mV amplitude of AC signal. The impedance characteristics were carried out by Solartron 1296 Dielectric interface and 1260 Impedance analyzer in a frequency range of 5 Hz-100 kHz at room temperature with a 50 mV amplitude of AC signal. These measurements were carried out by applying voltage to the bottom Pt electrode with the top Pt electrode grounded. The transfer characteristics (I_{DS}-V_G) and the output characteristics (I_{DS}-V_D) were measured by semiconductor parametric analyzer (Agilent 4155C).

3. Interface Charge Trap Density (D_{it}) of Metal-Insulator-Semiconductor Capacitor

For analysis of the interface trap, the equivalent circuit of a metal-insulator-semiconductor capacitor (MIS) is presented as Fig. 2(a) where C_D is capacitance of the depleted region of a semiconductor layer, $C_{it}(\omega)$ is the equivalent parallel interface trap capacitance, $G_p(\omega)$ is the equivalent parallel conductance and C_{ox} is the capacitance of an insulator layer. The admittance Y_s of the semiconductor portion is given by [20]

$$Y_s = j\omega C_D + C_{it}(2\tau_{it})^{-1}\left\{\ln\left[1 + (\omega\tau_{it})^2\right] + 2j\arctan(\omega\tau_{it})\right\} = j\omega C_p + G_p \quad (1)$$

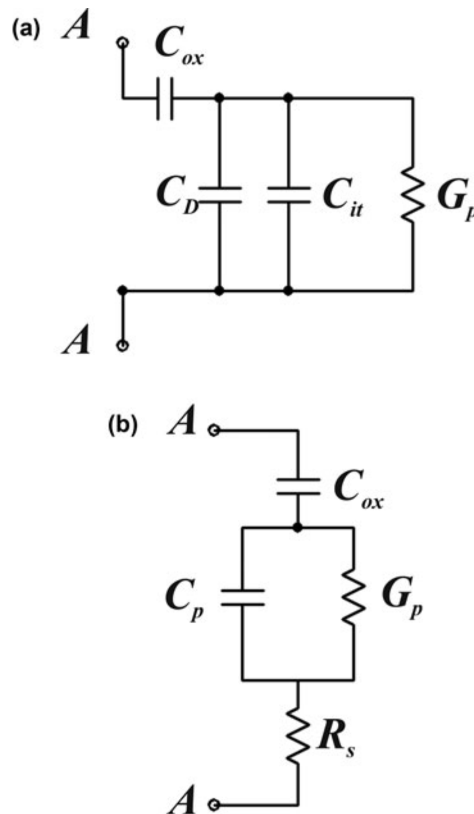

Figure 2. (a) Lumped parallel equivalent of circuit of MIS capacitor in depletion of a distribution of interface traps, (b) equivalent circuit of the MIS capacitor in depletion including series resistance R_s.

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where equivalent parallel capacitance C_p and conductance G_p of the semiconductor portion are defined as

$$C_p = C_D + C_{it}\,(\omega\tau_{it})^{-1}\arctan(\omega\tau_{it}) \tag{2}$$

and

$$\frac{G_p(\omega)}{\omega} = \frac{C_{it}}{2\omega\tau_{it}}\ln\left[1 + (\omega\tau_{it})^2\right] \tag{3}$$

respectively, where $C_{it} = qD_{it}$ is the interface trap capacitance measured at low frequencies, i.e., when $\omega\tau_{it} \ll 1$, and ω and τ_{it} are the angular frequency and the time constant of the interface charge trap, respectively. The peak value of the conductance loss G_p/ω equals to $0.4C_{it} = 0.4qD_{it}$ when $\omega\tau_{it} = 1.98$.

The value of G_p is not equal to the measured parallel conductance G_m. G_p can be extracted from the measured admittance, $Y_m = G_m + j\omega C_m$, corresponding to the equivalent circuit of Fig. 2(b) with C_m being the measured capacitance. Because of the existence of series resistance R_s, corrected capacitance C_c and corrected equivalent parallel conductance G_c will be calculated by

$$C_c = \frac{\left(G_m^2 + \omega^2 C_m^2\right) C_m}{a^2 + \omega^2 C_m^2} \tag{4}$$

and

$$G_c = \frac{\left(G_m^2 + \omega^2 C_m^2\right) a}{a^2 + \omega^2 C_m^2}, \tag{5}$$

respectively, where $a = G_m - \left(G_m^2 + \omega^2 C_m^2\right) R_s$ and $R_s = G_{ma}/\left(G_{ma}^2 + \omega^2 C_{ma}^2\right)$ with G_{ma} and C_{ma} being the capacitance and the equivalent parallel conductance at the accumulation region of MIS. Finally, the value of G_p/ω is given by

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_c}{G_c^2 + \omega^2 (C_{ox} - C_c)^2} \tag{6}$$

It is important to use the equation (6) to obtain G_p/ω rather than using G_m/ω to calculate D_{it} for MIS.

4. Results and Discussion

4.1. Ferroelectric Properties of PZT-Gate Insulator

Figure 3 shows the X-ray diffraction spectrum (XRD) of the PZT film. It is found that the PZT film presents a preferential orientation in the (111) direction due to the highly (111)-oriented Pt bottom electrode [23, 24]. Cross-sectional TEM image of this PZT film was shown in Fig. 5. It was observed that there were not any boundaries inside the PZT film; hence, this film was well crystallized from bottom to top [25].

Figure 4(a) shows the polarization-electric field (*P-E*) hysteresis of the Pt/PZT (170 nm)/Pt capacitor. This *P-E* loop has a good squareness. The obtained average remanent polarization (P_r) and average coercive field (E_c) of this PZT capacitor were 29 μC/cm^2 and 91 kV/cm, respectively, which is the typical P_r value of a PZT capacitor [25, 26]. In

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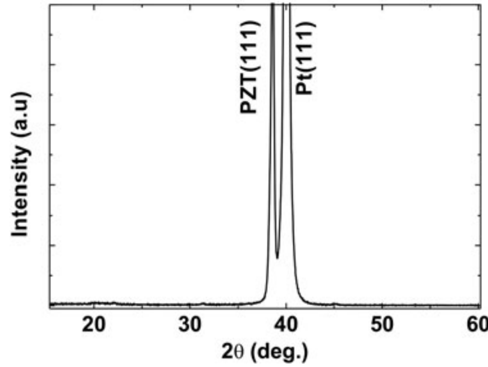

Figure 3. XRD spectrum of PZT film on Pt(111)/Ti/SiO_2/Si substrate.

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addition, the capacitance-voltage (C-V) characteristic of the PZT capacitor was measured and shown in Fig. 4(b), a butterfly shape of C-V characteristic was obtained because of natural ferroelectric properties of the PZT film. Furthermore, dielectric constant (ε) and loss tangent (tan δ) characteristics of this PZT capacitor were obtained by impedance measurement and shown in Fig. 4(c). It is recognized that the value of ε increased in the range of 600 to 700 with decreasing the frequency (F) because of the dipolar relaxation phenomenon [27]. The value of tan δ was as small as in $0.024 - 0.03$ range exhibiting a good quality of this PZT insulator. Because of the large value of P_r and the small loss tangent, this PZT film is suitable for a gate insulator for the FGT.

4.2. Electric Properties of Solution Processed Ferroelectric Gate Thin Film Transistor and Interface Charge Trap Density of ITO/PZT Structure

Figure 1(c) shows the schematic diagram of a FGT. Solution-process was used to fabricate PZT and ITO as a ferroelectric-insulator layer and a n-type channel, respectively. The cross-sectional TEM of the ITO/PZT/Pt structure is shown in Fig. 5(a). And high resolution TEM image of interfacial region between the ITO-channel and the gate PZT insulator is shown in Fig. 5(b). In this figure, the interface layer around 5 nm thickness was observed between ITO and PZT, which is similar to one of the FGT fabricated by the total solution process [18].

Figure 6(a) shows the I_{DS}-V_G characteristic of this device. The counter-clockwise hysteresis loop was obtained at the operation voltage of ± 7 V with the constant drain voltage (V_D) of 1.5 V due to natural ferroelectric properties of PZT gate-insulator. The obtained values of the on/off current ratio and the memory window were about 10^7 and 1.5 V, respectively. However, the 1.5 V-memory window is smaller than the theoretical value given by $2E_c d = 3.1$ V, where E_c and d are the coercive field and the thickness of the PZT film, respectively. Notably, the drain current at the gate voltage of -7 V was about 10^{-10} A despite of the large charge concentration around 10^{19} cm^{-3} of the ITO channel [18]. It means that the ITO channel was completely depleted by the huge polarization charge of the PZT gate-insulator. In addition, the subthreshold voltage swing was estimated to be 375 mV/decade. The field effect mobility of the channel, μ_{FE}, can be estimated in the

saturation region of I_{DS}-V_G curve as follows [15]

$$\mu_{FE} = \frac{\frac{\partial I_{DS}}{\partial V_G}\frac{\partial V_G}{\partial Q_{2D}}}{V_D\frac{W}{L}} \tag{7}$$

where Q_{2D} is the ferroelectric polarization and can be calculated as $Q_{2D} = P_r + C_{ox}V_G$ with C_{ox} being the capacitance of a ferroelectric capacitor; $\partial I_{DS}/\partial V_G$ was estimated from the I_{DS}-V_G curve at a saturation region, $\partial V_G/\partial Q_{2D} = 1/C_{ox}$ with $C_{ox} = 1.1\ \mu$F/cm^2 obtained

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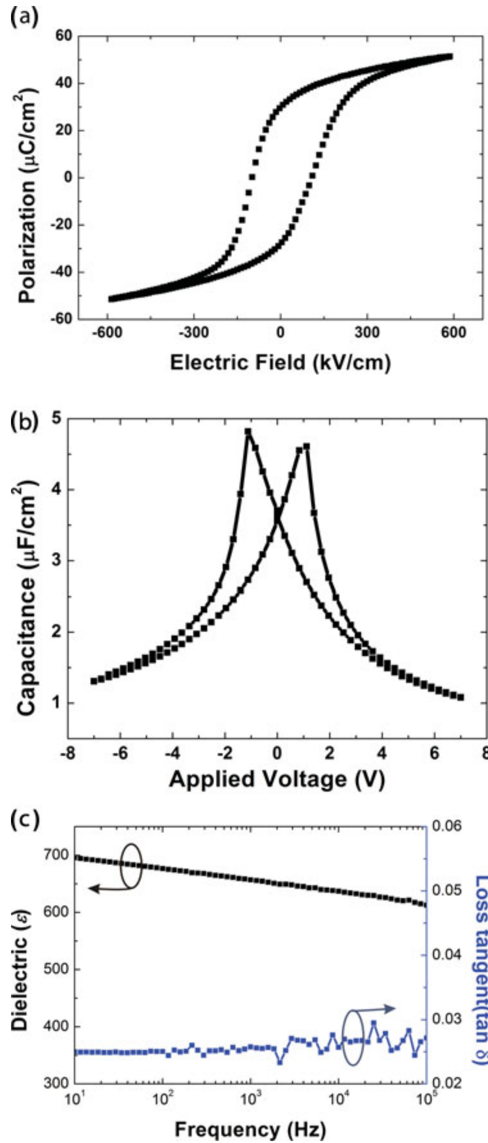

Figure 4. (a) *P-E* loop, (b) *C-V* characteristic, and (c) dielectric constant (ε) and loss tangent (*tan* δ) characteristics of MFM capacitor. (Figure available in color online.)

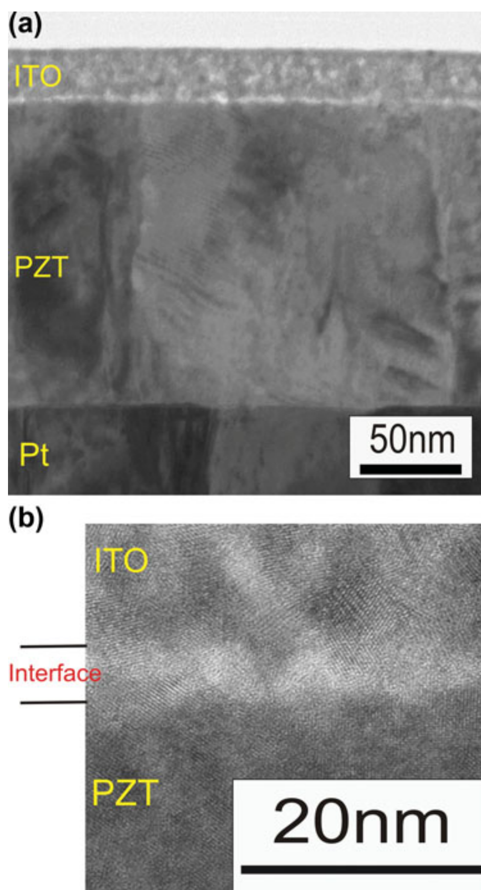

Figure 5. (a) Cross-sectional TEM image of ITO/PZT/Pt structure and (b) interface between ITO-channel and PZT film. (Figure available in color online.)

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from the capacitance-voltage (C-V) characteristic of the PZT capacitor [Fig. 4(b)] when $V_G = 7$ V. The value of μ_{FE} was estimated to be 7.9 cm^2/Vs, this value of μ_{FE} is comparable to those of the other TFTs using oxide semiconductors such as sputter ITO [14, 16], ZnO [28, 29], and IGZO [30].

Otherwise, the I_{DS}-V_D characteristics were carried out with the swept of V_D from 0 to 8 V, while V_G increased from 0 to 8 V [Fig. 6(b)]. It is recognized that a typical n-channel transistor operation was obtained with a large on current. With $V_D = V_G = 8$ V, the value of drain current was estimated to be 2.3 mA closing to one of the FGTs with the sputter ITO channels [14, 16]. Furthermore, the data retention property of this FGT was measured and the short retention property was confirmed to be about 10^3 s. It was suggested that the reason for the short retention property and the small memory window of this FGT could be attributed to the existence of a 5-nm-thick interface layer between ITO and PZT, which resulted in a large interface charge trap [18].

To further confirm the depletion and the accumulation characteristics of the ITO layer, C-V characteristic of the MFS capacitor, which is illustrated in Fig. 1(b), was investigated. The measured curve is shown as the curve (b) in Fig. 7. This C-V characteristic exhibited a

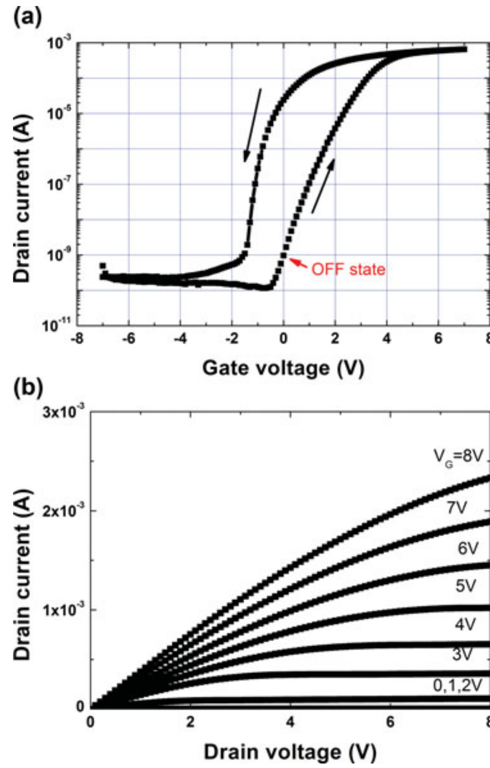

Figure 6. (a) I_{DS}-V_G characteristic and (b) I_{DS}-V_D characteristic of an FGT with 25-nm-thick ITO channel. (Figure available in color online.)

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large difference between negative and positive applied voltages. When the positive voltage was applied, the capacitance of MFS (C_{on}) behaved like a MFM capacitor indicating that the electrons were accumulated in the ITO layer; while at negative applied voltage, the capacitance of MFS (C_{off}) was much smaller than that of MFM as a result of the depletion of ITO layer [17]. This difference between C_{on} and C_{off} indicated that conductivity of ITO layer was wholly controlled by the huge polarization of the PZT film. That is the origin of ON/OFF operation of a FGT [31].

Next, impedance characteristic of MFS capacitor was carried out, and the admittance characteristic of this capacitor was also obtained. As the MFS capacitor can be considered like a MIS one when it is depleted as described above, it is expected that the interface charge trap density (D_{it}) of semiconductor (ITO)/insulator (PZT) contact could be estimated in this MFS capacitor. One of the problems lies in estimation of C_{ox}. Notably, the capacitance C_{ox} of the PZT film is the butterfly shape and its value depends on the value of applied voltage due to the natural ferroelectric property of the PZT film which is shown as the curve (a) in Fig. 7. In order to solve this problem, we should calculate the value of D_{it} at the applied voltage of 0 V corresponding to the OFF state at the depletion region of MFS in I_D-V_G of FGT, of which state is achieved when it was swept from −7 to 7 V.

Based on previous description, the value of G_p/ω depending on frequency of AC signal was calculated and plotted as the line (a) in Fig. 8 for the MFS capacitor. In this calculation, R_s was obtained from the impedance measurement of MFS capacitor at the accumulation

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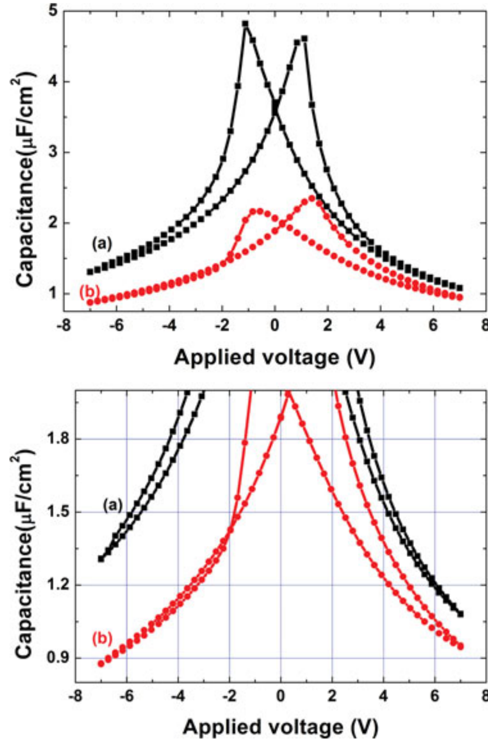

Figure 7. (a) *C-V* characteristics of MFM [line (a)] and MFS capacitors [line (b)]. (b) The zoom image of *C-V* characteristics. (Figure available in color online.)

state (ON state) of the MFS capacitor at the applied voltage of 5 V, C_{ox} was obtained from the impedance measurement of the MFM capacitor at the applied voltage of 0 V. Consequently, the value of C_{it} was obtained to be 2.08×10^{-9} F from the peak of G_p/ω which is clearly shown by the line (a) in Fig. 8. Hence, the interface charge trap D_{it} was estimated to be 1.2×10^{14} eV^{-1} cm^{-2}. Otherwise, by using the obtained value of C_{it} for

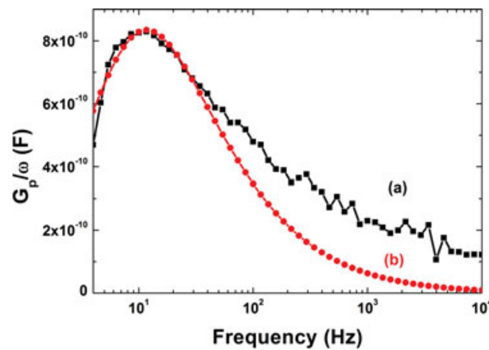

Figure 8. (a) G_p/ω vs. frequency (F) obtained from measured admittance, and (b) theoretical value of $G_p(\omega)/\omega$. (Figure available in color online.)

equation (3), the theoretical values of $G_p(\omega)/\omega$ were calculated and shown as a curve (b) in Fig. 8. This curve is close to the experimental curve of G_p/ω, which is a proof of validity of the calculation for D_{it}. The value of 1.2×10^{14} eV^{-1} cm^{-2} of D_{it} is several orders larger than those of MFIS [12] and MFMIS [6]. That can be attributed to the imperfect 5-nm-thick interface between ITO and PZT [Fig. 5(b)]. Therefore, this large value of D_{it} is pointed out as one of the major reasons for the short retention property of the FGT using ITO/PZT/Pt structure fabricated by a solution process. Moreover, that is also the reason for small memory window of 1.5 V of this FGT compared to the theoretical value of $2E_cd$ = 3.1 V. Hence, we insist it is inevitably necessary to improve the interface between a semiconductor channel and a gate-insulator layer to obtain better performances of FGT such as long retention, large on/off current ratio and large memory window. As a matter of fact, Y. Kato *et al*. reported the good performances of FGT such as a long retention time and a high on/off current ratio of 10^5 because of the very good interface of the epitaxial ZnO/PZT structure fabricated by the pulsed laser deposition technique [17].

5. Conclusion

In this work, an FGT using ITO/PZT/Pt structure was fabricated. The obtained values of the on/off current ratio, the memory window and the subthreshold voltage swing were about 10^7, 1.5 V and 375 mV/decade, respectively. The *C-V* characteristic of MFS capacitor confirmed that the conductivity of ITO layer was wholly controlled by the huge polarization of PZT-gate insulator which is the origin of on/off operation of FGTs. Therefore the MFS capacitor can be considered as a MIS one when it is depleted. That means a conductance method could be applied to extract D_{it} in the MFS capacitor. Based on this consideration, the interface charge trap D_{it} in the MFS capacitor fabricated by solution process was obtained to be 1.2×10^{14} eV^{-1} cm^{-2} by using conductance. The large value of D_{it} is due to the imperfect interface of 5-nm-thickness between ITO and PZT observed by HR-TEM. This large D_{it} can be considered as one of the major reasons both of the short retention properties and the small memory window of 1.5 V of the FGT.

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