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Low-temperature PZT thin-film ferroelectric memories fabricated on SiO$_2$/Si and glass substrates

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A B S T R A C T

In a ferroelectric-gate thin film transistor memory (FGT) type structure, the gate-insulator layer is extremely important for inducing the charge when accumulating or depleting. We concentrated on the application of low-temperature PZT films crystallized at 450, 500 and 550 °C, instead of at conventional high temperatures ($\geq$600 °C). Investigation of the crystalline structure and electrical properties indicated that the PZT film, crystallized at 500 °C, was suitable for FGT fabrication because of a high (111) orientation, large remnant polarization of 38 μC/cm^2 on SiO$_2$/Si substrate and 17.8 μC/cm^2 on glass, and low leakage current of 10^{-6} A/cm^2. In sequence, we successfully fabricated FGT with all processes below 500 °C on a glass substrate, whose operation exhibits a memory window of 4 V, ON/OFF current ratio of 10^5, field-effect mobility of 0.092 cm^2 V^{-1} s^{-1}, and retention time of 1 h.

1. Introduction

The search for low-temperature ($\leq$500 °C) production processes of electronic devices has increased in recent years due to the promising possibility of low cost and light production of high-density integrated circuits on flexible substrates (polymers or metal foils), instead of traditional silicon substrates [1–3]. For instance, when embedding a ferroelectric memory device on silicon-based CMOS integrated circuits, the temperature processing is required to be lower than 450 °C [4]. A ferroelectric-gate field-effect transistor (denoted as FGT), which uses ferroelectric material as the gate-insulator layer and an oxide-semiconductor material as a channel layer, is of extensive interest for nonvolatile memory applications because it possesses a simple memory-cell structure and low-power consumption in principle [5–7]. Unfortunately, the difficulty of lowering temperature processing of the FGT is lodged in the ferroelectric-gate insulator layer. As it is well known, when the FGT uses an organic ferroelectric-gate insulator layer, all processing temperatures could be reduced as low as 200 °C. However, the operation of such an FGT requires a high writing/reading voltage (>10 V) to polarize the insulating layer, which leads to high power consumption. Moreover, the performance of organic FGTs is very

sensitive to the fabrication process [8,9]. Accordingly, from the point-of-view of power consumption and high reproducibility, an inorganic ferroelectric-gate insulator layer is superior to an organic one.

Among inorganic ferroelectric materials, lead zirconate titanate (PZT) is the primary option for fabricating FGTs on non-based silicon substrates. PZT satisfies the constraint on processing temperature ($\leq$600 °C), which is lower compared to other inorganic ferroelectrics such as strontium bismuth tantalate ($\geq$700 °C) [10], and bismuth lathanum titanate ($\geq$650 °C) [11]. Many works have reported a success of growing high-quality PZT films below 500 °C from chemical vapor deposition, including tailoring precursor solution [12–14], seeding the film [15,16], hydrothermal annealing [17,18], and better lattice matching [19].

At this time, we are not aware of any reports on the fabrication of FGTs using inorganic ferroelectric materials processed at or below 500 °C. The reason for this lies not only on the temperature process of the ferroelectric-gate insulator layer, but depends on the oxide-semiconductor channel layer. Previously, a high-quality PZT film deposited by a solution process at a temperature $\leq$500 °C has been achieved [20]. Alternatively, using the solution-processed ITO channel at 450 °C, a clear operation of a FGT has been demonstrated. However, a 600 °C PZT film was used in this case and the FGT was fabricated on a single-crystal STO (111) substrate [21]. Therefore, in this study, a combination of the two processes mentioned above has been proposed in order to realize a FGT with

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all processes below 500 °C and fabricated on SiO_2 (500 nm)/Si substrate or glass.

2. Experimental

A preliminary experiment was performed to find the optimum condition for preparing high-quality, low-temperature PZT films. First, a 100-nm-thick Pt film followed by a10-nm-thick Ti film was deposited on SiO_2 (500 nm)/Si and glass substrates by using rf sputtering at temperature of 100 °C. Second, a ferroelectric-gate PZT film with 160-nm thickness was deposited after a sol−gel coating of an alkoxide-based 8.0wt% $Pb_{1.2}Zr_{0.4}Ti_{0.6}O_3$ precursor solution (Mitsubishi Materials) and then crystallized at 450, 500 and 550 °C for 30 min in a pure-air atmosphere using a rapid thermal annealing furnace (RTA, ULVAC-Mila5000). To evaluate the electrical properties of the PZT films, we prepared Pt/PZT/Pt capacitor structure with area of $100 \times 100 \ \mu m^2$ as shown in Fig. 1(a). Fig. 1(b) shows the FGT structure with a flat-gate electrode fabricated on the SiO_2 (500 nm)/Si substrate. In this step, the source and drain regions were patterned after a conventional photolithography process, rf sputter deposition of 50-nm-thick Pt film, and lift-off process. Using this technique, the gap of the FGT was precisely created that was 5 μm in length. Third, the channel layer was formed from a 20-nm-thick ITO film, which was deposited by a sol−gel coating of a carboxylate-based ITO precursor solution (5.0 wt% SnO_2 doped; Kojundo Kagaku) and crystallized at 450 °C for 20 min in air. After that, the ITO layer was etched by an inductively coupled plasma (ICP) method with the assistance of photolithography in order to pattern the channel with a width of 60 μm. Fig. 1(c) shows the FGT structure with a patterned gate of 50 μm in length, which is different with the flat-gate structure of Fig. 1(b) and fabricated on glass.

The shape of the gate, the source-drain and the channel areas of the patterned-gate FGT on the glass substrate were observed by an optical microscope. The crystalline property of the PZT films on the $Pt/Ti/SiO_2$/Si substrates was confirmed by X-ray diffraction. The electrical properties of the PZT films, such as polarization-voltage (*P-V*) and leakage current-voltage (*I-V*) characteristics, were measured at a frequency of 1 kHz by using the Sawyer−Tower method. The transfer (I_D-V_{GS}) and output (I_D-V_{DS}) characteristics of the fabricated FGTs were measured by means of a semiconductor parametric analyzer (Agilent 4155C).

3. Results and discussion

The crystalline structure of the PZT films formed on $Pt/TiO_2/SiO_2$/Si substrates at various annealing temperatures of 450, 500 and 550 °C is shown in Fig. 2. Well crystallized, preferentially oriented (111)-PZT films are found on the three samples. It is likely

that the high (111) texture of the PZT films partly originates from the Pt seed layer, which has a face-centered cubic structure also with a high degree of (111) texture. Furthermore, in our previous research, a new route was found to obtain high-quality PZT films even at 450 °C, under a strict process of nitrogen gas control or carbon retained before annealing, in order to avoid the formation of the pyrochlore phase, which usually leads to a high temperature of perovskite phase formation [20]. From Fig. 2, one can see that the (111) peak intensity of the PZT films increases with annealing temperature. This is reasonable considering an earlier report; where a highly crystallized PZT film is usually obtained when the annealing temperature is approaches 600 °C [22].

Fig. 3(a) shows the polarization-voltage (*P-V*) hysteresis loops of the PZT films formed on $Pt/TiO_2/SiO_2$/Si substrates at various annealing temperatures of 450, 500 and 550 °C, which were measured by applying a sine wave voltage with amplitude changing from −10 V to 10 V. The hysteresis loops have a well-saturated behavior and an obvious squareness, which are consistent with the highly (111)-oriented PZT films, as indicated from Fig. 2. For all cases, the remnant polarization (*Pr*) and twice coercive voltages (*2Ec*) are approximated from each loop at different annealing temperatures. For instance, the 500 °C PZT film had a *Pr* and *2Ec* of about 38 $\mu C/cm^2$ and 2 V, respectively. These values match with the ones reported previously [20], and are comparable to those from other works, of which the crystallization temperature of PZT film is 600 °C or higher [21,22]. Fig. 3 (b) shows the dependence of the leakage current on the applied voltage for the PZT films corresponding to the hysteresis loops shown in Fig. 3(a), which were measured from 0 to 10 V. It is interesting that at an applied voltage of >3 V, the leakage current of the 500 °C PZT film is lower than that of the 450 and 550 °C PZT films. In particular, the leakage current is
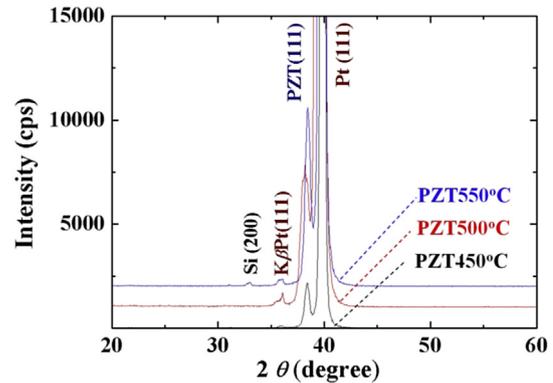
Fig. 2. XRD patterns for the PZT films crystallized at 450, 500 and 550 °C on SiO_2/Si substrates.
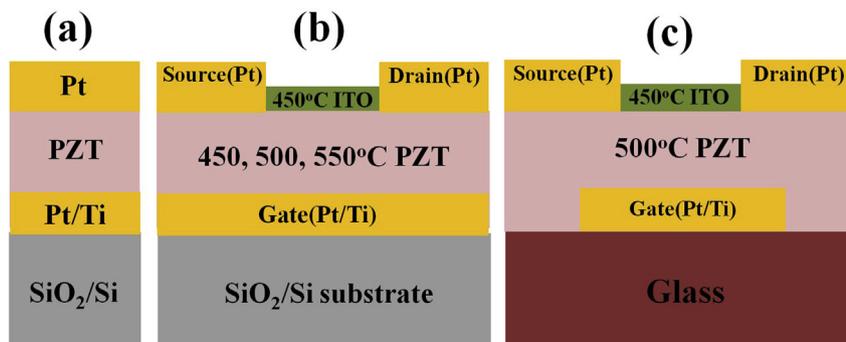
Fig. 1. Schematic drawing: (a) Pt/PZT/Pt capacitor structure, (b) flat-gate FGT fabricated on SiO_2/Si substrate and (c) patterned-gate FGT fabricated on glass substrate.
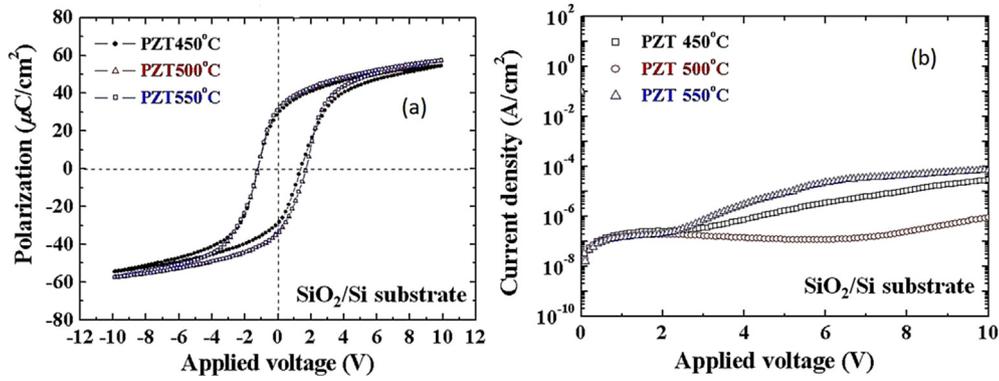
Fig. 3. Electrical properties of the PZT films crystallized at 450, 500 and 550 °C: (a) polarization-voltage hysteresis loops and (b) leakage current-voltage characteristics.

determined to be about 10^{-6} A/cm^2, even at an applied voltage of 10 V, which is one or two orders of magnitude lower than the other samples. According to the result, it is supposed that the 500 °C PZT film is mostly acceptable for ferroelectric memory application.

Fig. 4 shows the transfer characteristics of FGTs with a flat gate fabricated on SiO$_2$/Si substrates, with the PZT gate insulator crystallized at 450, 500 and 550 °C. These flat-gate FGTs have a channel length of 5 μm and channel width of 60 μm. In the measurement, the gate voltage (V_{GS}) was gradually swept from -7 V to 7 V with a step of 0.1 V, and the bias voltage between the drain and source (V_{DS}) was kept at a constant 1.5 V. It is clear that the transfer characteristics imply a memory functionality with a counterclockwise hysteresis loop, typical n-type transistor, whose the ON/OFF current ratio was in range of 10^6–10^7, and the memory window was almost 2 V for all cases, which are equal to the $2V_c$ estimated from Fig. 3. That is, a well-formed interface between the ITO channel layer and PZT gate-insulator layer might be achieved using the low temperature processes. It can be seen from this figure that higher ON current saturation is correlated with higher annealing temperatures. Unfortunately, the OFF current also increases when the annealing temperature increases. Therefore, considering the results obtained in Figs. 3 and 4, the 500 °C PZT film is expected to be the best selection for FGT fabrication on glass, because it has the lowest leakage current and better transfer characteristics as compared to the other cases.

Fig. 5 shows an optical microscope image of the FGT patterned on glass. Note that cross-section view of the FGT structure on glass is schematically drawn in Fig. 1(c). For this patterned-gate FGT fabrication, all processes have temperatures equal or lower than

500 °C. According to this image, one can determine that the channel length is 5 μm, the channel width is 60 μm, and the gate length is 50 μm. Fig. 6(a) and (b) show hysteresis loops and leakage current characteristics of the 500 °C PZT film measured directly on the FGT area, for which the source and drain areas were simultaneously connected to ground while the gate was connected to the pulsed voltage before forming the channel layer. The PZT film has a large coercive voltage of 4 V, which is favorable for the wide memory margin requirement and a remnant polarization of 17.8 μC/cm^2 at an applied voltage of 8 V, which is large enough for clarifying the ON- and OFF-state of the memory. Here, we calculate the capacitance per unit area unit of the gate insulator $C_{ox} = P/V$, and find $C_{ox} = 2.2$ μCV^{-1} cm^{-2}. From Fig. 6(b), a low leakage current density of $<10^{-5}$ A/cm^2 at an applied voltage of 8 V is achieved, which supports that the 500 °C PZT film deposited on glass still remains an adequate ferroelectric for FGT fabrication.

Fig. 7 points out the operation of the low-temperature FGT on glass. From Fig. 7(a), the transfer characteristic of FGT clearly describes a memory function with memory window of 4 V and ON/OFF current ratio of 5 orders of magnitude. Once again, the $2E_c$ of P-V loop shown in Fig. 6(a) and the memory window shown in Fig. 7(a) are similar from each other. In addition, one can obtain from Fig. 7(a) that the gate leakage current is on the order of nA, which supports a low power consumption in the stand-by state. Fig. 7(b) shows the output characteristics of the FGT fabricated on glass, when the V_{DS} was continuously scanned from 1 to 8 V and the V_{GS} was varied from 1 to 8 V with an incremental step of 1 V. It can be seen that the drain current has a
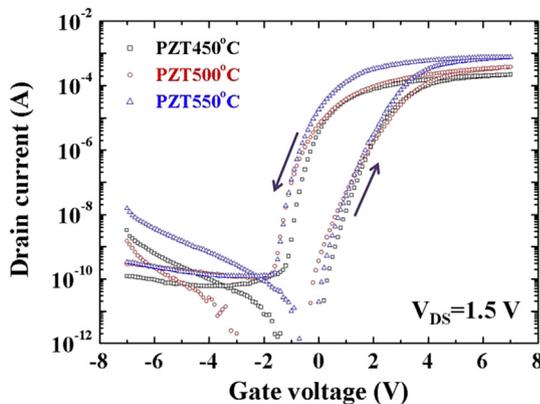

Fig. 4. Transfer characteristics of flat-gate FGTs fabricated on SiO$_2$/Si substrates, whose PZT gate insulator crystallized at 450, 500 and 550 °C.
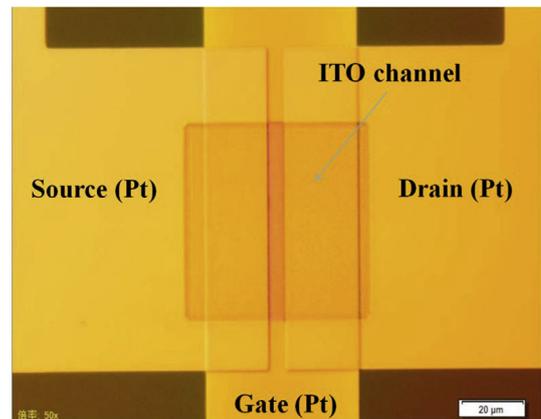

Fig. 5. Optical microscope image of the FGT patterned on a glass substrate whose channel length is 5 μm, channel width is 60 μm, and gate length is 50 μm.
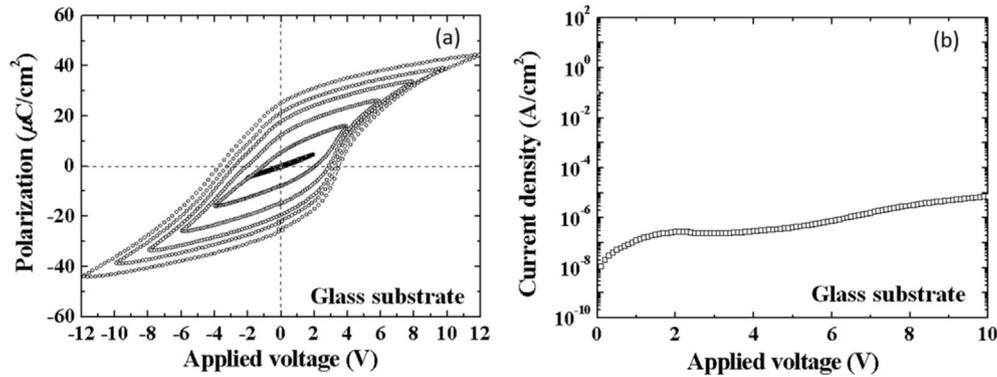
Fig. 6. Electrical properties of the PZT film crystallized at 500 °C on glass substrate: (a) polarization-voltage hysteresis loops and (b) leakage current-voltage characteristic.
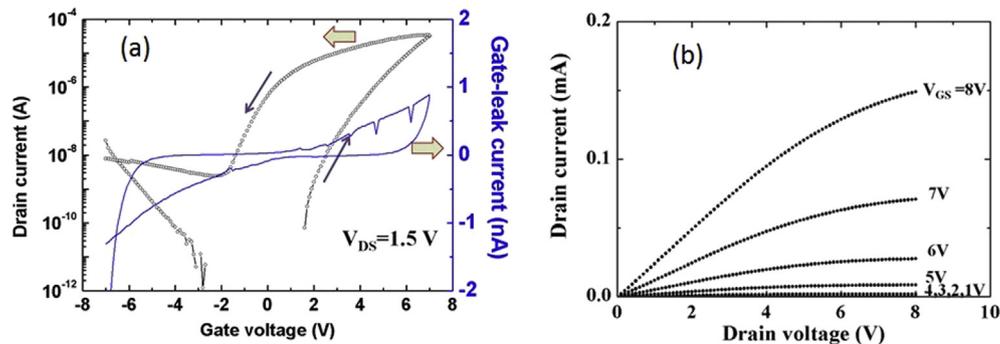

Fig. 7. (a) Transfer, gate leak and (b) output characteristics of FGT with a patterned gate fabricated on glass, whose channel length, channel width and gate length are 5 μm, 60 μm and 50 μm, respectively.

hard saturation, reaching a magnitude of 0.15 mA with $V_{GS} = V_{DS} = 8$ V. Although the saturated ON drain current (I_D) is not very high as compared to the other cases [23,24], it will promote further investigations to obtain a higher level without any amplifiers by processing the ITO/PZT interface or by improving the PZT film quality. The field-effect mobility (μ_{FE}) is calculated from the saturation region of Fig. 7(b) by using the formula: $\mu_{FE} = I_D[(W_{DS}/2L_{DS})C_{ox} \cdot (V_{GS} - V_T)^2]^{-1}$, where $I_D = 0.15$ mA, the $L_{DS} = 5$ μm, $W_{DS} = 60$ μm, $C_{ox} = 2.2$ μCV^{-1} cm^{-2}, $V_{GS} = 8$ V, $V_T = 1.5$ V. Using these parameters, we estimated μ_{FE} to be 0.092 cm^2 V^{-1} s^{-1}. This value is much lower than the other reports on the high-temperature FGT [23,24], but it is almost comparable to an amorphous silicon TFT [25].

Fig. 8 shows the retention characteristics of the FGT fabricated on glass substrate. In this measurement, the ON and OFF states were, in turn, written by using a square pulse with amplitudes of $+6$ V and -6 V at a frequency of 1 kHz. The stored memory states were kept at room temperature and they were read out by using $V_{DS} = 1.5$ V and $V_G = 6$ V at each waiting time of 10^4 s. One can see from Fig. 8 that the ON/OFF current ratio is almost unchanged even after 1 h, but degraded quickly after longer time storage. Although the obtained retention time of a solution-process FGT with all processes below 500 °C is much shorter than the commercial requirement of about 10 years for non-volatile memory devices, it supports a promising future research to improve the retention characteristics from the viewpoint of low temperature processes for a better formation of ITO/PZT interface, comparing with the conventional Si-based ferroelectric memories [26–29]. Further investigation on the ITO/PZT interface would be analyzed, and La-based materials might be used as a capping layer in order to
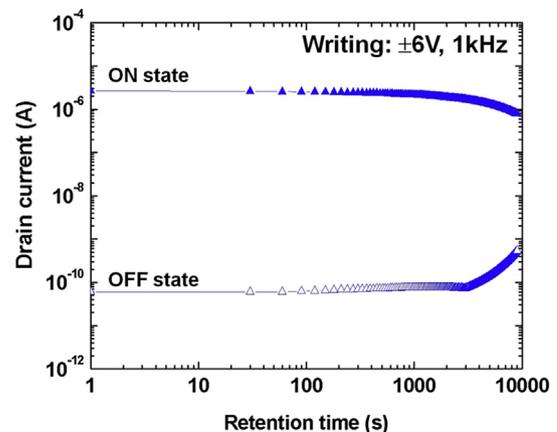

Fig. 8. Retention characteristics of the FGT patterned on glass substrate, in which a square pulse of ±6 V with a frequency of 1 kHz was used for data writing.

prevent diffusion of Pb from the PZT film to the ITO film, which will improve the retention characteristics [30,31].

4. Conclusions

We have investigated the crystalline and electrical properties of PZT films processed at 450, 500 and 550 °C. It is found that although the crystalline quality of 500 °C PZT film is worse than that of 550 °C PZT film, it has the lowest leakage current of 10^{-6} A/cm^2 and a better transfer characteristic when fabricating FGT on SiO$_2$(500 nm)/Si substrate. Using the 500 °C processed PZT film, the

FGT with channel length of 5 μm, channel width of 60 μm, and gate length of 50 μm was successfully fabricated on glass. As a result, for the first time, we verify that the memory window, ON/OFF current ratio, field-effect mobility and the retention time of the FGT were 4 V, 10^5, 0.092 cm^2 V^{-1} s^{-1}, and 1 h, respectively.

Acknowledgment

References

[1] H. Akinaga, Recent advances and future prospects in functional-oxide nano-electronics: the emerging materials and novel functionalities that are accelerating semiconductor device research and development, Jpn, J. Appl. Phys. 52 (2013) 100001−100200.

[2] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors, Nature 432 (2004) 488−492.

[3] I.D. Kim, M.H. Lim, K.T. Kang, H.G. Kim, S.Y. Choi, Room temperature fabricated ZnO thin film transistor using high-K Bi$_{1.5}$Zn$_{1.0}$Nb$_{1.5}$O$_7$ gate insulator prepared by sputtering, Appl. Phys. Lett. 89 (2006) 022905−022907.

[4] P. Muralt, R.G. Polcawich, S. Trolier-McKinstry, Piezoelectric thin films for sensors, actuators, and energy harvesting, MRS Bull. 34 (2009) 658−664.

[5] J.F. Scott, C.A. Paz de Araujo, Ferroelectric memories, Science 246 (1989) 1400−1405.

[6] J.L. Moll, Y. Tarui, A new solid state memory resistor, IEEE Trans Electron Devices 10 (1963) 338.

[7] H. Ishiwara, Proposal of adaptive-learning neuron circuits with ferroelectric analog-memory weights, Jpn. J. Appl. Phys. 32 (1993) 442−446.

[8] Y.J. Park, H.J. Jeong, J. Chang, S.J. Kang, C. Park, Recent development in polymer ferroelectric field effect transistor memory, Semicond. Sci. Technol. 8 (2008) 51−65.

[9] C.H. Park, S. Im, J. Yun, G.H. Lee, B.H. Lee, M.M. Sung, Transparent photostable ZnO nonvolatile memory transistor with ferroelectric polymer and sputter-deposited oxide gate, Appl. Phys. Lett. 95 (2009) 223506.

[10] W.S. Yang, S.J. Yeom, N.K. Kim, S.Y. Kweon, J.S. Roh, Effects of crystallization annealing sequence for SrBi$_2$Ta$_2$O$_9$ (SBT) film on Pt/SBT interface morphology and electrical properties of ferroelectric capacitor, Jpn. J. Appl. Phys. 39 (2000) 5465−5468.

[11] M.C. Kao, H.Z. Chen, S.L. Young, Ferroelectric properties and leakage current mechanisms of Bi$_{3.25}$La$_{0.75}$Ti$_3$O$_{12}$ thin films with a-axis preferred orientation prepared by sol−gel method, Mater. Lett. 62 (2008) 629−632.

[12] J. Perez, P.M. Vilarinho, A.L. Kholkin, High-quality PbZr$_{0.52}$Ti$_{0.48}$O$_3$ films prepared by modified sol−gel route at low temperature, Thin Solid Films 449 (2004) 20−24.

[13] K. Maki, B.T. Liu, Y. So, H. Vu, R. Ramesh, J. Finder, Z. Yu, R. Droopad, K. Eisenbeiser, Low-temperature fabrication of epitaxial and random-oriented Pb(Zr,Ti)O$_3$ capacitors with SrRuO$_3$ electrodes on Si wafers, Integr. Ferroelectr. 52 (2003) 19−31.

[14] M. Mandeljc, M. Kosec, B. Malic, Z. Samardzija, Contribution to the low-temperature crystallization of pzt-based csd thin films, Integr. Ferroelectr. 36 (2001) 163−172.

[15] C.K. Kwok, S.B. Desu, Low temperature perovskite formation of lead zirconate titanate thin films by a seeding process, Mater. Res. 8 (1993) 339−344.

[16] A. Wu, P.M. Vilarinho, I. Reaney, I.M.M. Salvado, Early stages of crystallization of sol−gel-derived lead zirconate titanate thin films, Chem. Mater 15 (2003) 1147−1155.

[17] Z. Wei, K. Yamashita, M. Okuyama, Preparation of Pb(Zr$_{0.52}$TiO$_{0.48}$)O$_3$ thin films at low-temperature of less than 400°C by hydrothermal treatment following sol-gel deposition, Jpn. J. Appl. Phys. 40 (2001) 5539−5542.

[18] C.H. Lu, W.J. Hwang, Y.C. Sun, Ferroelectric lead zirconate titanate thin films synthesized via a high-pressure crystallization process, Jpn. J. Appl. Phys. 41 (2002) 6674−6678.

[19] I.D. Kim, H.G. Kim, Characterization of highly preferred Pb(Zr,Ti)O$_3$ thin films on La$_{0.5}$Sr$_{0.5}$CoO$_3$ and LaNi$_{0.6}$Co$_{0.4}$O$_3$ electrodes prepared at low temperature, Jpn. J. Appl. Phys. 40 (2001) 2357−2362.

[20] J. Li, H. Kameda, B.N.Q. Trinh, T. Miyasako, P.T. Tue, E. Tokumitsu, T. Mitani, T. Shimoda, A low-temperature crystallization path for device-quality ferroelectric films,, Appl. Phys. Lett. 97 (2010) 102905−103101.

[21] T. Miyasako, B.N.Q. Trinh, M. Onoue, T. Kaneda, P.T. Tue, E. Tokumitsu, T. Shimoda, Ferroelectric-gate thin-film transistor fabricated by total solution deposition process, Jpn. J. Appl. Phys. 50 (2011) 04DD09.

[22] S.Y. Chen, I.W. Chen, Texture development, microstructure evolution, and crystallization of chemically derived PZT thin films, J. Am. Ceram. Soc. 81 (1998) 97−105.

[23] E. Tokumitsu, M. Senoo, T. Miyasako, Use of ferroelectric gate insulator for thin film transistors with ITO channel, Microelectron. Eng. 80 (2005) 305−308.

[24] T. Miyasako, M. Senoo, E. Tokumits u, Ferroelectric-gate thin-film transistors using indium-tin-oxide channel with large charge controllability, Appl. Phys. Lett. 86 (2005) 162902−162904.

[25] H. Uchida, K. Takechi, S. Nishida, S. Kaneko, High-mobility and high-stability a-Si:H thin film transistors with smooth SiN$_x$/a-Si interface, Jpn. J. Appl. Phys. 30 (1991) 3691−3694.

[26] J.M. Benedetto, R.A. Moore, F.B. McLean, Effects of operating conditions on the fast-decay component of the retained polarization in lead zirconate titanate thin films, J. Appl. Phys. 75 (1994) 460−466.

[27] K.W. Lee, W.J. Lee, Relaxation of remanent polarization in Pb(Zr,Ti)O$_3$ thin film capacitors, Jpn. J. Appl. Phys. 41 (2002) 6718−6723.

[28] T.P. Ma, J.P. Han, Why is nonvolatile ferroelectric memory field-effect transistor still elusive? IEEE Electron Device Lett. 23 (2002) 386−388.

[29] C.T. Black, C. Farrell, T.J. Licata, Suppression of ferroelectric polarization by an adjustable depolarization field, Appl. Phys. Lett. 71 (1997) 2041−2043.

[30] G.D. Wilk, R.M. Wallace, J.M. Anthony, High-κ gate dielectrics: current status and materials properties considerations, J. Appl. Phys. 89 (2001) 5243−5275.

[31] T.P.C. Juan, C.L. Lin, W.C. Shih, C.C. Yang, J.Y.M. Lee, D.C. Shye, J.H. Lu, Fabrication and characterization of metal-ferroelectric PbZr$_{0.6}$Ti$_{0.4}$O$_3$ insulator La$_2$O$_3$ -semiconductor capacitors for nonvolatile memory applications, J. Appl. Phys. 105 (2009) 061625.