

A 60 GHz CMOS Power Amplifier for Wireless Communications

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ABSTRACT

This paper presents a 60 GHz power amplifier (PA) suitable for wireless communications. The two-stage wideband PA is fabricated in 55 nm CMOS. Measurement results show that the PA obtains a peak gain of 16 dB over a -3 dB bandwidth from 57 GHz to 67 GHz. It archives an output 1 dB compression point (OP1dB) of 4 dBm and a peak power added efficiency (PAE) of 12.6%. The PA consumes a total DC power of 38.3 mW from a 1.2 V supply voltage while its core occupies a chip area of 0.45 mm².

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INTRODUCTION

Wireless communications using the millimeter-wave band have been growing in the past few years due to its high data-rate transmission capability. The demands for high data-rate short range wireless communication have attracted a great deal of interest in the design of 60 GHz systems. As a result, the Federal Communications Commission (FCC) of the United States has officially approved the spectrum utilization for 57 GHz to 64 GHz for commercial use. CMOS PA is among the most challenging building blocks in implementing a 60 GHz system. The main purpose of a PA design is to provide sufficiently high output power, while another important target is to achieve high efficiency. There are several obstacles which make the implementations of a PA very difficult in CMOS technology. The use of submicron CMOS increases the difficulty of implementation due to technology limitations such as low breakdown voltage and poor transconductance. The linearity and power efficiency are lower than other technologies. However, with the trend of lower power transmitters in the next generation, implementation of CMOS PAs with good efficiencies are becoming realistic despite steadily declining field-effect transistor (FET) breakdown voltages.

In this paper, we are going to present the designs and measurement results of a 60 GHz PA targeted for wireless communications. The paper is organized as follows. Section 2 presents fundamentals of power amplifiers. Section 3 introduces the architecture of the proposed 60 GHz PA including a detailed description of the circuit topology. The measurement results are presented in section 4 and conclusions are given in the last section.

POWER AMPLIFIER BASICS

PA Block Diagram

The general design concept of a PA is given in Fig. 1. The two port network is applied in the design consisting of two matching networks that are used on both sides of the power transistor. Maximum gain will be realized when the matching networks provide a conjugate match between the source/load impedance and the transistor impedances [1]. Specifically, the matching networks transform the input and output impedances Z_0 to the source and load impedances Z_S and Z_L , respectively. Both input and output matching networks are designed for 50 Ω external load.

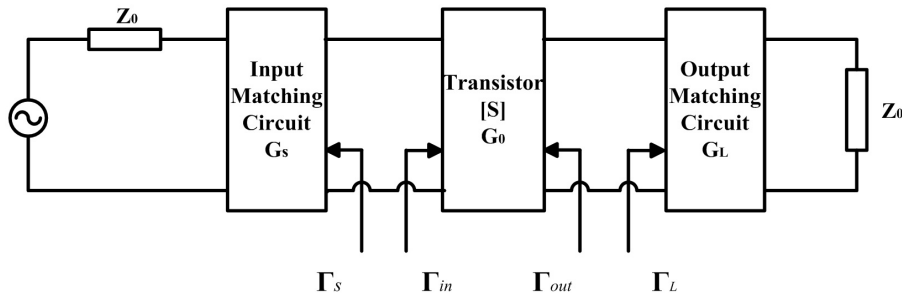


Figure 1. Block diagram of a PA.

Table 1. Conduction angles of the different current-mode PA classes

Class	Conductance Angle
A	2π
AB	$\pi-2\pi$
B	π
C	$0-\pi$

Classification of PAs

There are generally two types of PAs: the current source mode PA and the switching mode PA. Different kinds of each mode of PAs and their functional principles are introduced in detail in [2]. In the current source mode PA, the power device is regarded as a current source, which is controlled by the input signal. The most important current source mode PAs are class A, class B, class AB and class C. They differ from each other in the operating point. Fig. 2 illustrates the different classes of the current source mode PA in the transfer characteristic of a FET device. The drain current I_D exhibits pinch-off, when the channel is completely closed by the gate-source voltage V_{GS} and reaches the saturation, in which further increase of gate-source voltage results in no further increase in drain current. The other very important concept to define the different classes of the current source mode PA is the conduction angle α . The conduction angle depicts the proportion of the RF cycle for which conduction occurs. The conduction angles of different classes are summarized in table 1.

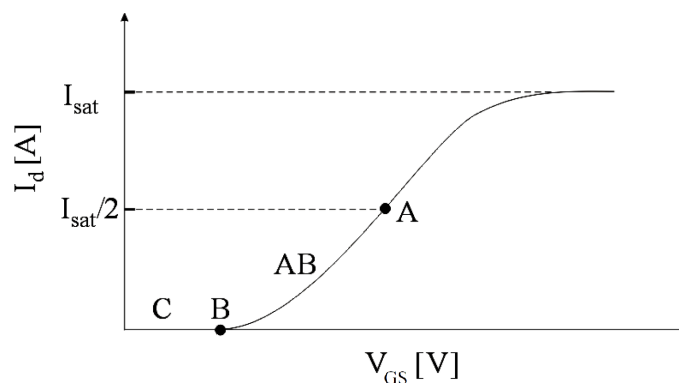


Figure 2. Operating points of different current-mode PAs classes.

PA Efficiency

Efficiency is a measure of performance of a PA. The performance of a PA will be better if its efficiency is higher, irrespective of its definition. The PA is the most power-consuming block in a wireless transceiver. Its power efficiency has a direct impact on the battery life of mobile devices. Several definitions of efficiency are commonly used with PAs. Most widely used measures are the drain efficiency and power added efficiency. The drain efficiency

is defined as

$$\eta = \frac{P_{\text{OUT}}}{P_{\text{DC}}} \quad (1)$$

where P_{OUT} is the RF output power at operating frequency and P_{DC} the DC power consumption of the PA output stage. It reveals how efficient the PA is when it converts the power from DC to AC. The PAE is given by

$$\text{PAE} = \frac{P_{\text{OUT}} - P_{\text{IN}}}{P_{\text{DC}}} \quad (2)$$

where P_{IN} is the input power fed to the PA and P_{DC} the total DC power consumption of the PA. The PAE gets close to η if the gain of the PA is sufficient high so that the input power is negligible.

DESIGN OF 60 GHz POWER AMPLIFIER

The 60 GHz PA is designed using 55 nm CMOS process provided by Fujitsu Ltd. Its back end consists of 11 copper layers and a top aluminum redistribution layer (RDL). The cross-view of a grounded coplanar wave-guide transmission line (GCPW-TL) is depicted in Fig. 3 [3]. The GCPW-TL with the characteristic impedance of 50Ω (the 50Ω GCPW-TL) is used for shunt and series stubs of the matching networks and for connecting to the input and output pads of the 60 GHz PA. Its signal line consists of the RDL layer with a width of $8 \mu\text{m}$. Ground (GND) walls composed of the 6th to 11th metal layers with a width of $9 \mu\text{m}$ are placed on the both side of the signal line at the distance of $11.5 \mu\text{m}$. The 3rd to 5th metal layers are meshed and stitched together with vias to form the GND plane. The

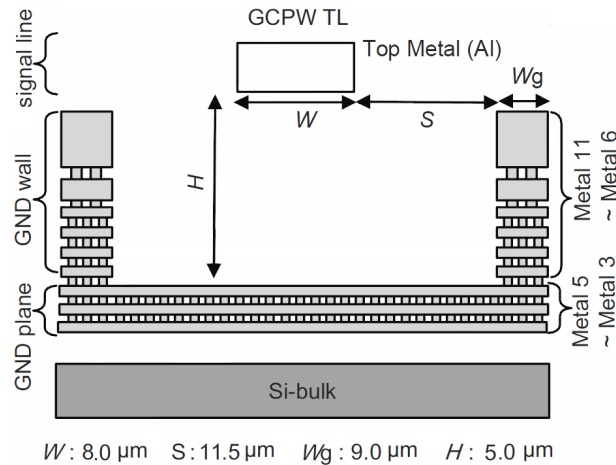


Figure 3. The cross-view of the 50Ω GCPW-TL.

The complete circuit of the proposed PA with all component values are given in Fig. 4. It includes an input matching network, an output matching network, two common-source based amplifying stages and an inter-stage matching network. For bandwidth enhancement, multi-stage matchings using capacitors and GCPW-TLs are adopted. The series capacitors and GCPW-TLs form 4th-order and 2nd-order high-pass filters at the input and output of the PA, respectively. The input is matched to 50Ω for measurement purpose while the load is optimized for maximizing output power using load-pull simulation. The inter-stage matching network is based on the PI network for wideband performance. A 128Ω resistor is added in series to the transistor's gate of the first amplifying stage for stabilization. The minimum-loss cascade stabilizing resistor value is determined from the Smith chart by finding the constant resistance that is tangent to the appropriate stability circle [4]. All of the capacitors also act as coupling capacitors while the DC bias voltages are applied through the shunt GCPW-TLs. The bias voltages are common to all amplifying stages. The connection between the MOSFETs, MOM capacitors and GCPW-TLs are made by the 10th and 11th metal layers. The lengths of the GCPW-TLs and the MOM capacitor values are determined by a nonmetric optimization process taking into account the models of MOSFETs, MOM capacitors and GCPW-TLs. The parasitic components are extracted using bond-based design which is a measurement-based design approach to avoiding the difficulty associated with layout parasitics when ordinary layout parasitic extraction (LPE) tools used for chip design do not extract inductances [5]. The far end of each shunt stub is terminated by a wideband decoupling power line with very low characteristic impedance (the 0Ω TL) [6].

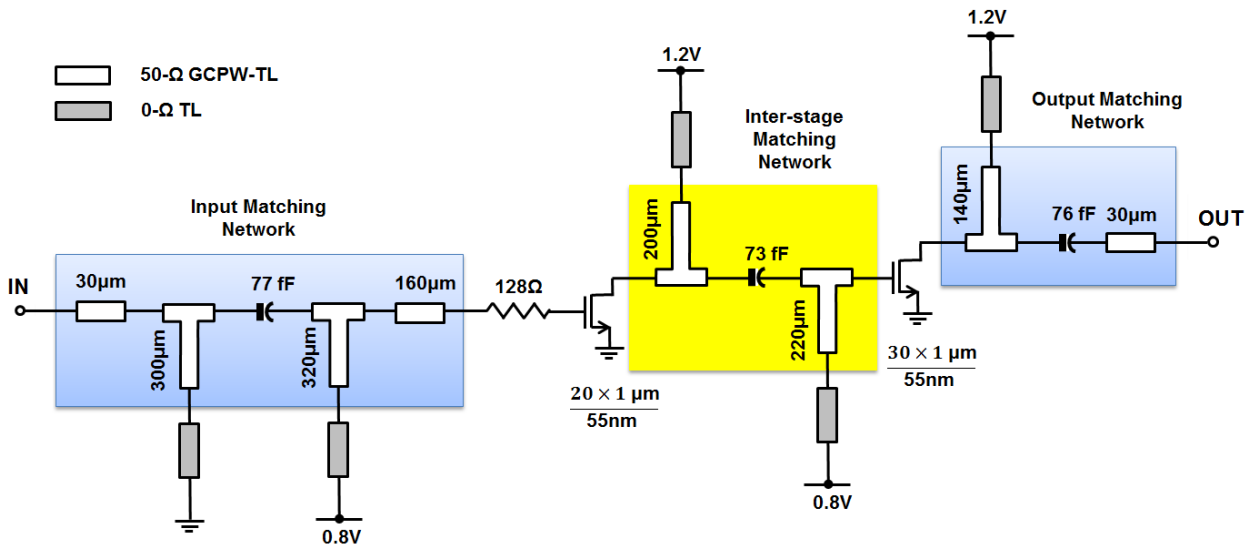


Figure 4. The proposed 60 GHz PA.

MEASUREMENT RESULTS

In order to verify the performance of the 60 GHz PA, a chip prototype was fabricated in 55 nm CMOS. Fig. 5 shows the die microphotograph of the PA. The PA occupies an area of $0.72 \times 0.63 \text{ mm}^2$ including probe pads. The PA was measured by means of on-chip probings using a probe station. The RF probe pads were designed for ground-signal-ground (GSG) probes with $750 \mu\text{m}$ pitch. The Anritsu 37397D VNA and V-band frequency extenders were used for measuring small-signal S-parameters.

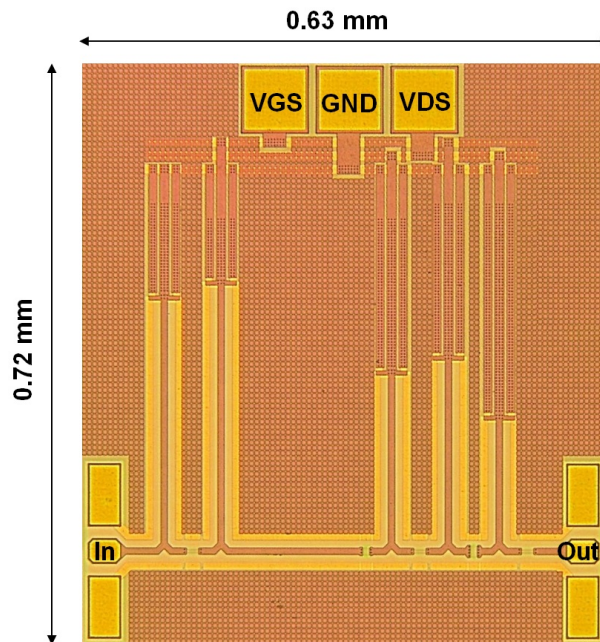


Figure 5. The die microphotograph of the 60 GHz PA.

Fig. 6 shows the measured and simulated S-parameters of the 60 GHz PA. As can be seen in this figure, the measured results show good agreements with the simulated ones. Both input and output return loss indicate wideband performance when S_{11} and S_{22} remain below -10 dB over almost of the -3 dB bandwidth from 57 GHz to 67 GHz . The 60 GHz PA achieves a peak gain of 16 dB at 61 GHz . The reverse isolation is lower than -20 dB (not shown in the figure). A high reverse isolation guarantees high stability for the PA.

Fig. 7 plots the output power versus the input power. A Keysight E8244A signal generator and a VivaTech

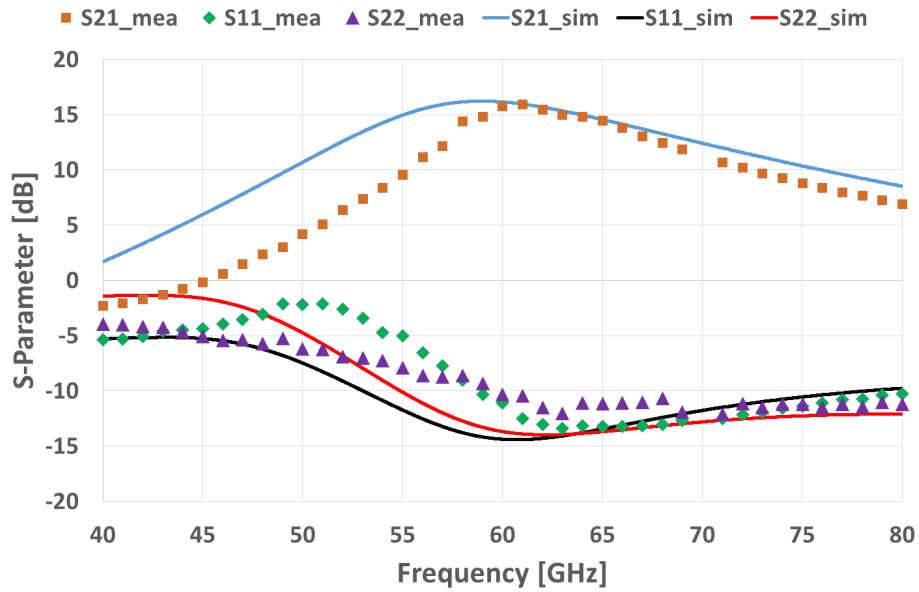


Figure 6. The measured and simulated S-parameter of the 60 GHz PA.

VTXFA-06-12 signal module were used for generating input signal at 60 GHz while a VDI PM5-305V power sensor was used to measure the output power. Due to the equipment limitation at V-band in our laboratory, the output power can only be measured up to -3 dBm of the input power. At 60 GHz, the designed PA obtains a OP1dB of approximately 4 dBm. Fig. 8 and Fig. 9 show the drain efficiency and PAE versus the input powers, respectively. The designed PA archives a peak PAE of 12.6% at -3.5 dBm input power. The PA consumes a total power of 38.3 mW from a 1.2 V supply voltage. Table 2 summarizes the performance of the proposed PA and compares it to other published ones operating in the similar frequency range. A popular figure-of-merit (FoM) used for comparison is defined as the gain bandwidth product (GBWP) divided by the DC power consumption (P_{DC}).

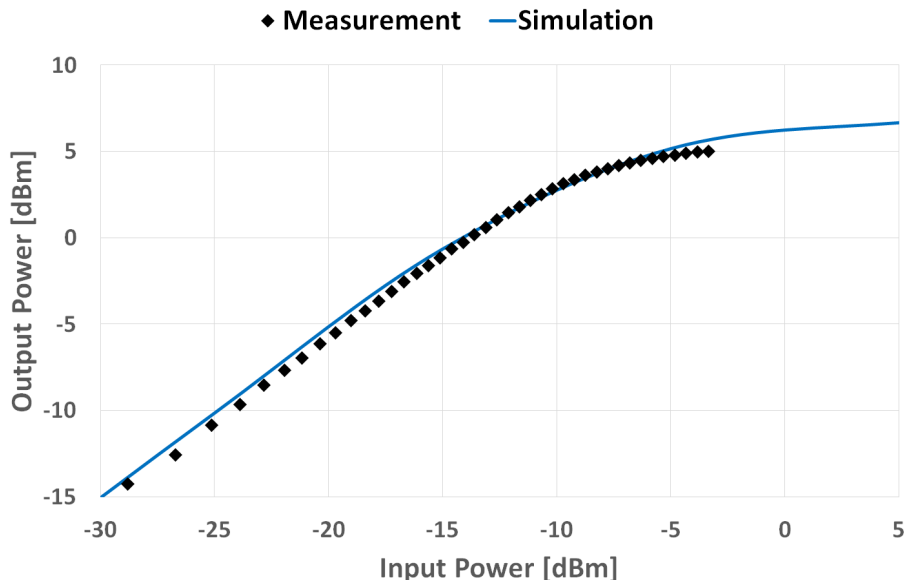


Figure 7. The measured and simulated output power versus the input power of the 60 GHz PA.

CONCLUSIONS

In this paper, we have presented the designs and measurement results of the 60 GHz PA targeted for wireless communications. The proposed PA obtains the peak gain of 16 dB while the -3 dB bandwidth cover the entire of the

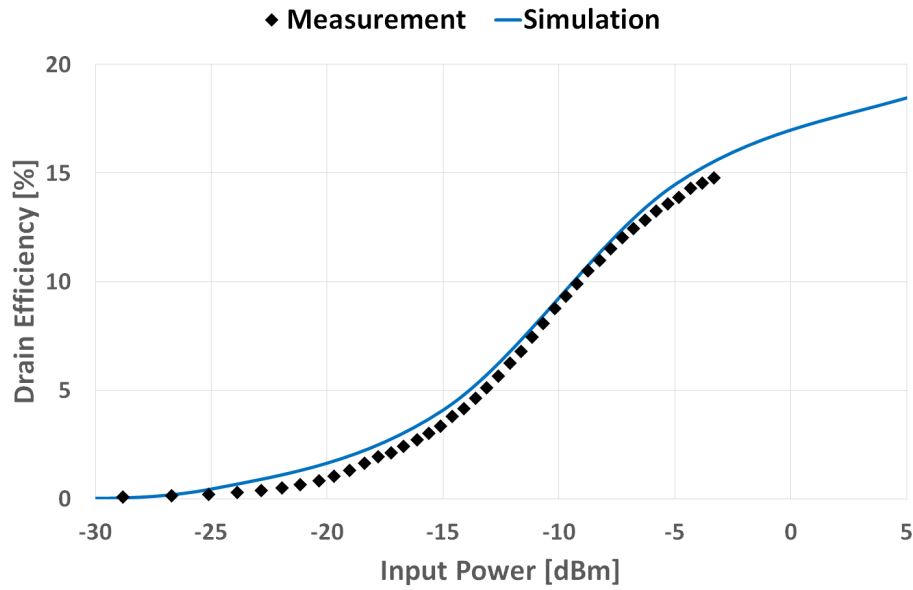


Figure 8. The measured and simulated drain efficiency of the 60 GHz PA.

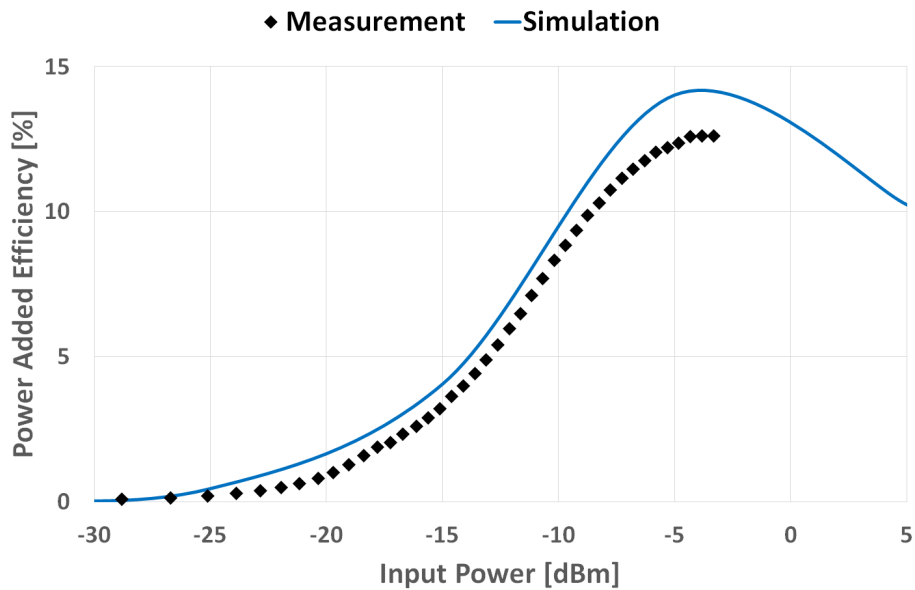


Figure 9. The measured and simulated PAE of the 60 GHz PA.

Table 2. Comparison with previous published PAs operating in the 60 GHz frequency band

Parameter	RFIC' 10 [7]	APMC' 12 [8]	RFIT' 15 [9]	T-MTT' 13 [10]	MWCL' 15 [11]	This work
CMOS Technology	65 nm	65 nm	65 nm	65 nm	65 nm	55 nm
No. of Stages	3	2	3	4	3	2
Gain (dB)	30	12.1	20	20	20	16
-3 dB BW(GHz)	7	7	8	4.5	15	10
Peak PAE (%)	18	11.1	14	6.6	9	12.6
Die Area (mm ²)	0.06	0.61	0.56	2.25	0.7	0.45
OP1dB (dBm)	6.8	4.5	10.4	13.5	5	4
Power Cons. (mW)	65	45.8	93	480	60	38.3
GBWP/ P_{DC}	3.41	0.62	0.86	0.09	2.5	1.65

60 GHz frequency band. It exhibits the OP1dB of 4 dBm and the peak PAE of 12.6%. The total power consumption of the PA is 38.3 mW while it occupies the chip area of 0.45 mm² including probe pads. The performances of the designed PA are competitive to other state-of-the-art PAs in CMOS.

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BIOGRAPHY OF AUTHORS



Tuan Anh Vu received the B.S degree and M.Sc degree in Electronics and Telecommunications Technology from University of Engineering and Technology, Vietnam National University in 2006 and 2009, respectively. In 2013, he received Ph.D degree in the field of analog/mixed-signal RF nanoelectronics from University of Oslo, Norway. Since 2014, he has been a lecturer at Faculty of Electronics and Telecommunications, VNU University of Engineering and Technology. Dr. Tuan Anh Vu was with Department of Semiconductor Electronics and Integration Science, Hiroshima University as a postdoctoral researcher for one year. He is now doing postdoc at Department of Electrical and Computer Engineering, University of California, Davis. His research interests are analog RF integrated circuit designs including power amplifiers, low noise amplifiers, mixers, frequency multipliers, etc.