

FABRICATION OF FERRITE-BASED INTEGRATED MICRO-INDUCTORS ONTO SILICON WAFER

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Abstract. In this work, the technology for fabricating integrated micro-inductors onto silicon is developed. The paper will report the experimental process and technology development to fabricate the micro-inductor on-to silicon substrates with the hybrid integration approach. Copper is used for the fabrication of the conductor windings and vias. Electro-deposition is chosen for depositing copper. Via is electro-deposited to make the connection between bottom tracks and top tracks. The ferrite core is fabricated and sintered from in-house ferrites or commercial ferrite films.

Keywords: Integrated micro-inductor, ferrite, integration.

1. Introduction

Integrated inductors are important passive components for power supplies on chip, a lot of research was done to make them small enough and with high performances: high power density and high efficiency [1]. This work aims to fabricate inductors on-to silicon with low profile (less than 250 μm) and small size (less than 4 mm^2) which should be used for power conversion (approximately 1 W) working at medium frequencies (5 to 10 MHz). NiZn ferrites are chosen for making the magnetic core thanks to their moderate permeability and high resistivity stable at the medium frequencies. In hybrid integration approach, the magnetic core is fabricated individually and then placed on copper wires. In final micro-devices, the two levels of windings are bonded with the technology of thick photoresist mold. The solutions and technologies are described in this article. In hybrid approach, magnetic cores can be either printed by screen printing or cut from commercial films, then sintered. Bottom Cu windings are electro-deposited on wafers and planarized by photoresist. Cores are stacked on bottom windings. Two copper tracks on-to silicon

should be bonded by flip-chip technique [2]. Figure 1 shows schematically fabrication steps when windings are completed by using thick photo-resist mold technology. The detail of process development will be described in following sections.

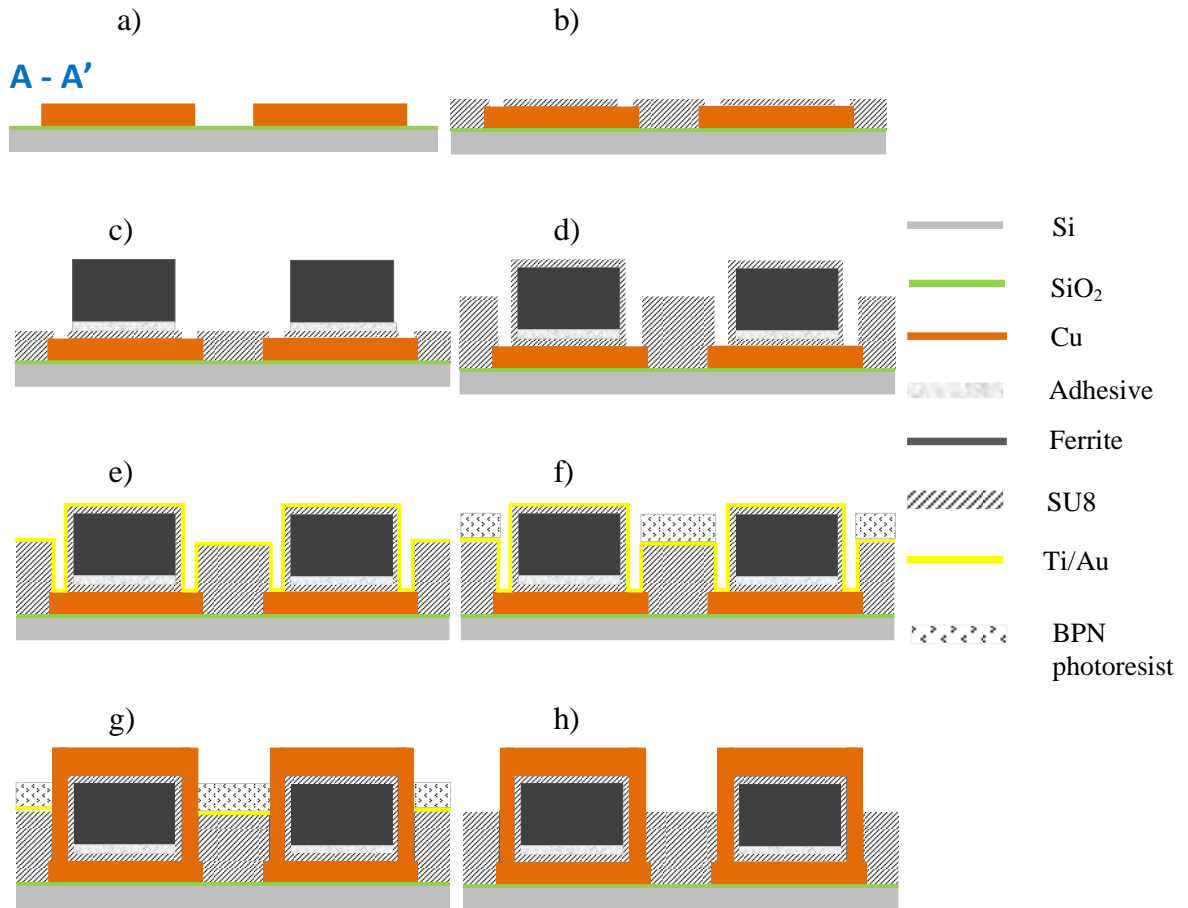


Figure 1. Fabrication processes *a) Electroplating bottom windings on wafer, b) Planarization of tracks, opening vias c) Glueing cores on bottom windings d) Covering cores, opening vias e) Sputtering seed layers f) Preparing photoresist mold g) Depositing top windings and vias h) Removing photoresist residues and seed layers*

2. Content

In hybrid integration, cores are made from in-house ferrites as printed cores and from commercial ferrite tapes as cut cores [3]. The copper windings are deposited by thick photoresist mold technology with SU8 and Bump Plating Negative (BPN) photoresist [2]. The micro-inductor was fabricated and Figure 1 shows the schematic of processes.

- Step 1: Electroplating bottom windings on Si/SiO₂ wafer.

The 500nm-thick SiO₂ layer insulates the inductor from the wafer. So as to electroplate bottom windings, Ti (50nm)/Au (100nm) seed layers are prepared on the

Si/SiO₂ wafer by physical vapor deposition (PVD) technique. Photolithography technique is used to create photoresist patterned layer of 50µm on the wafer. 50 µm-thick bottom tracks are deposited and then, the seed layers of Au and Ti are removed by KI + I₂ solution and solution of HF.

- Step 2: Bottom windings planarization and opening vias

The 50 µm-thick bottom tracks are covered by a layer of SU8 sprayed on top with the smallest thickness. We will characterize that photoresist layer with the cross section of the final inductor. Vias are opened by photolithography technique, as shown in Figure 2.

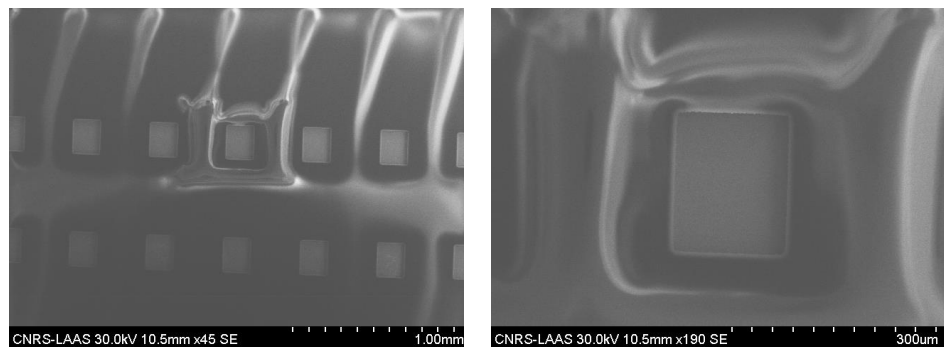


Figure 2. *Opened vias on the bottom tracks*

- Step 3: Glueing cores on bottom windings by the machine Tresky 3000 with Epoteck® 353NDT (as shown in Figure 3).

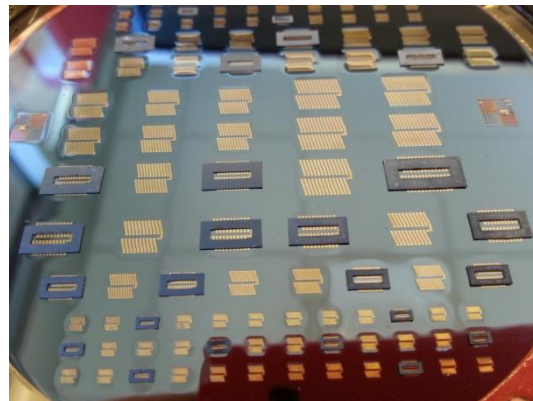


Figure 3. *Fixed cores on bottom windings*

- Step 4: Covering cores by photoresist and opening vias

SU8 photoresist is covered on the glued cores. We will characterize the inductor's cross section to measure the thickness of this layer. Then, we use photolithography technique to open vias.

- Step 5: Sputtering seed layers, preparing mold of photoresist

We deposit seed layers of Ti (50nm)/Au (100nm) and the problem of bubbles occurred as shown in Figure 4 and Figure 5. The residue of photoresist can be seen when the bubble was wrecked. That is as a result of the air under the stacked cores, which expanded due to the heat created in the wafer during the process of metallization, and then, evacuated to the surface in the form of bubbles. The bubble problem occurred more probably near cores. We use the BPN photoresist to prepare mold layer on top of seed layers. And the next step is electro-deposition of the top windings and vias.

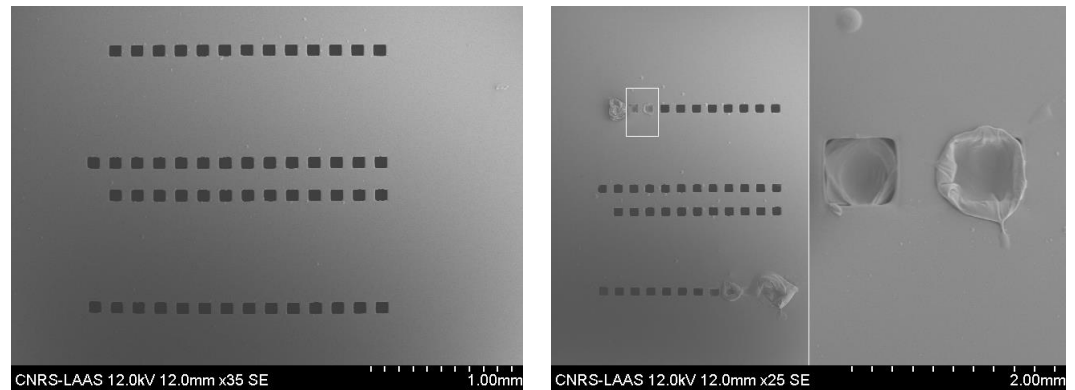


Figure 4. Problem of bubble in air-core inductor (on the right image)

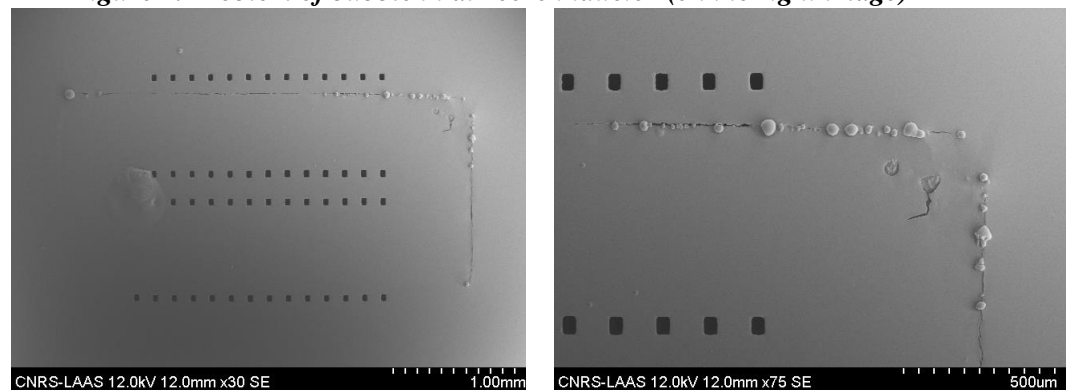


Figure 5. Problem of bubbles in ferrite-core inductor

- Step 6: Electroplating top windings and vias

We electroplate top windings and vias simultaneously in the photoresist patterned layer. After that we remove the photoresist residue and layers of Ti/Au. Figure 6 shows the final inductor.

With the purpose of characterization, we cut the final inductor with A-A', B-B' and C-C' guide lines. The cross sections matching to the cutting lines were observed by scanning electron microscope (SEM). The shape of copper vias can be seen in Figure 7. We can observe good Cu-via-Cu connections at some places and besides, several bad connections. The inductor device may have the problem of open circuit with the bad

connections. We can observe the topology of the printed core in Figure 8 which is thicker near the border. Ferrite core is about $156\ \mu\text{m}$ thick corresponding to the cutting line C-C'. Electroplated bottom winding is $60\ \mu\text{m}$ thick and the thickness of the top winding is $50\ \mu\text{m}$. The total thickness of the inductor is $370\ \mu\text{m}$. The first and the second SU8 layer is about $70\ \mu\text{m}$ and $35\ \mu\text{m}$ thick (as shown in Figure 9). The resistance of a final inductor is measured $125\ \text{m}\Omega$ up to $90\ \text{MHz}$.

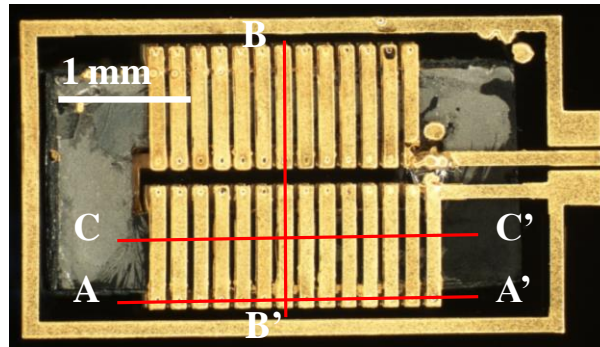


Figure 6. The realized ferrite-core micro-inductor with the cutting guide lines

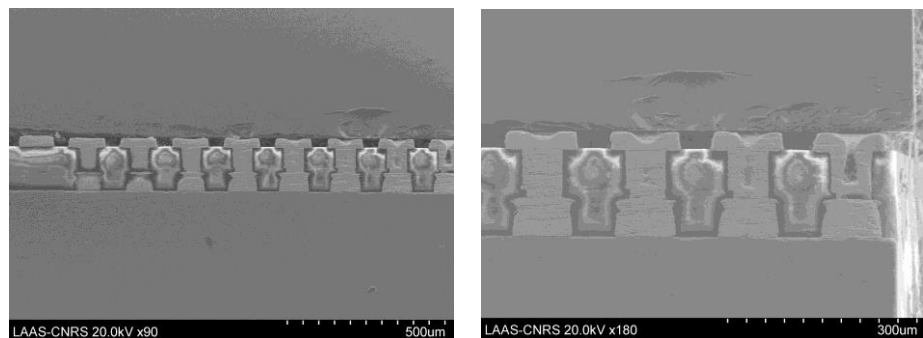


Figure 7. A-A' cutting line and the cross section of the inductor with vias

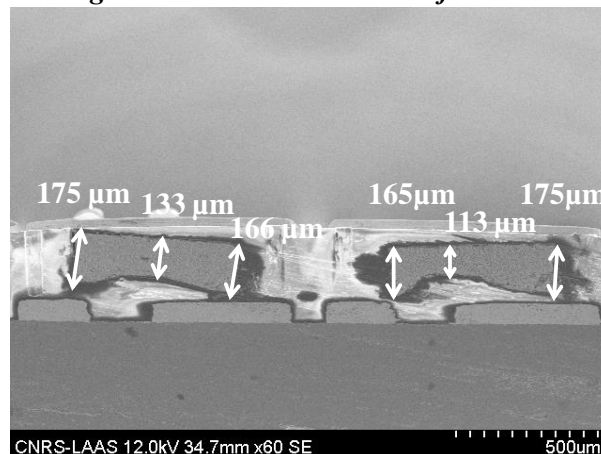


Figure 8. B-B' cutting line and the cross section of the inductor with the ferrite core

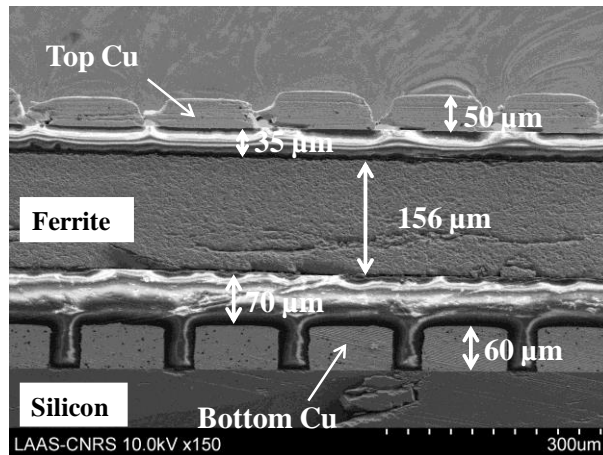


Figure 9. C-C' cutting line and the cross section of the inductor with bottom and top windings, ferrite core and photoresist layers

3. Conclusions

Ferrite-based micro inductors were fabricated. The air-core inductor resistance is about 125 mΩ up to 90 MHz. Ferrite-core inductors have poor electrical connection in conductor windings due to bubble problems. That should be solved by improving the process of sticking core. We can improve the winding connection by polishing of copper tracks and make flip-bonding a successful process.

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REFERENCES

- [1] C. O. Mathuna, N. Wang, S. Kulkarni, and S. Roy, 2012. *Review of Integrated Magnetics for Power Supply on Chip (PwrSoC)*. IEEE Transactions on Power Electronics, 27 (11).
- [2] D. Bourrier, M. Dilhan, A. Ghannam, and H. Granier, 2011. *Comparisons of the new thick negative resist to SU8 resist*. Conference on Micromachining and Microfabrication Process Technology XIII, San Jose, CA, 7972.
- [3] Y. M. Nguyen, M. Brunet, J. P. Laur, D. Bourrier, S. Charlot, Z. Valdez-Nava, V. Bley and C. Combettes, 2013. *Low-profile small-size ferrite cores for powerSiP integrated inductors* Power Electronics and Applications. (EPE), 15th European Conference (IEEE, Lille) pp 1-7.