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Si-doping effect on solution-processed In-O thin-film transistors

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Ha Hoang[1], Tatsuki Hori[1], To-oru Yasuda[2], Takio Kizu[3], Kazuhito Tsukagoshi[3], Toshihide Nabatame[4], Bui Nguyen Quoc Trinh[5,6] and Akihiko Fujiwara[1,2]

[1] Department of Physics, School of Science and Technology, Kwansei Gakuin University, 2-1 Gakuen, Sanda, Hyogo 669-1337, Japan
[2] Department of Nanotechnology for Sustainable Energy, School of Science and Technology, Kwansei Gakuin University, 2-1 Gakuen, Sanda, Hyogo 669-1337, Japan
[3] International Center for Materials Nanoarchitectonics (WPI-MANA), National Institute for Materials Science (NIMS), 1-1 Namiki, Tsukuba, Ibaraki 305-0044, Japan
[4] MANA Foundry and MANA Advanced Device Materials Group, National Institute for Materials Science (NIMS), 1-1 Namiki, Tsukuba, Ibaraki 305-0044, Japan
[5] Faculty of Engineering Physics and Nanotechnology, VNU University of Engineering and Technology, Vietnam National University, 144 Xuan Thuy, Cau Giay, Hanoi, Vietnam
[6] Nanotechnology Program, VNU Vietnam Japan University, Vietnam National University, Luu Huu Phuoc, Nam Tu Liem, Hanoi, Vietnam

E-mail: akihiko.fujiwara@kwansei.ac.jp

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Abstract

In this work, silicon-doped indium oxide thin-film transistors (TFTs) have been fabricated for the first time by a solution processing method. By varying the Si concentration in the In_2O_3–SiO_2 binary oxide structure up to 15 at%, the thicknesses, densities, and crystallinity of the resulting In–Si–O (ISO) thin films were investigated by x-ray reflectivity (XRR) and x-ray diffraction techniques, while the produced TFTs were characterized by a conventional three-probe method. The results of XRR analysis revealed that the increase in the content of Si dopant increased the thickness of the produced film and reduced its density, and that all the Si-doped ISO thin films contained only a single amorphous phase even after annealing at temperatures as high as 800 °C. The manufactured ISO TFTs exhibited a reduction in the absolute value of threshold voltage V_T close to 0 V and low current in the off-state, as compared to those of the non-doped indium oxide films, due to the reduced number of oxygen defects, which was consistent with the behavior of ISO TFTs fabricated by a sputtering method. The ISO TFT with a Si content of 3 at% annealed at 400 °C demonstrated the smallest subthreshold swing of 0.5 V/dec, V_T of −5 V, mobility of 0.21 $cm^2 V^{-1}s^{-1}$, and on/off current ratio of about 2×10^7.

1. Introduction

Recently, metal oxide semiconductors have attracted significant attention as potential materials for the next-generation electronic devices due to their high carrier mobility and optical transparency. In particular, doped indium oxides (In–O: IO) have been studied as channel materials for thin-film transistors (TFTs) that can be used in high-definition flat panel displays, owing to the excellent device characteristics of amorphous In-Ga-Zn-O compounds [1–3]. However, their resistance against external stress and scale-up capabilities require further improvement [2–5].

Because Si doping is able to effectively stabilize the amorphous structures of IO films and reduce the number of oxygen deficiencies due to the high dissociation energy of the Si−O bond, it can be potentially used for the reduction of a large negative threshold voltage V_T [6–9]. Therefore, Si-doped IO (In–Si–O: ISO) is a promising material for the fabrication of TFTs utilized in flat panel displays. Multiple studies on ISO and its properties were performed in the past [6, 10, 11]; however, no solution-processed ISO transistors have been reported yet. Using a spin coating method, the concentration of doped Si species can be easily changed by varying its content in solution, which allows investigation of the doping effect over a wide range of dopant concentration despite the slight reduction in the film quality. In this respect, spin coating is advantageous to another typical ISO deposition

method, DC sputtering, which requires fabrication of separate targets for each studied composition. Moreover, spin coating is a very practical method as compared to physical vapor deposition, because of its simplicity, low cost, easy control over chemical stoichiometry, and applicability to mass production [12–18]. In addition, a relatively large variety of substrates, including glass and plastic, can be utilized for solution processing.

Regarding to patterning, it is important to isolate each transistor to reduce the gate leak current and minimize the crosstalk between various devices. Lithography represents a widely used patterning technique, which, however, requires long processing times as well as the use of complicated procedures and special facilities such as cleanrooms. In contrast, a patterning technique based on the wetting properties of a material is expected to be much easier to implement [19–21]. To ensure good wetting, a hydrophobic surface must be matched with a non-polar solution, and a hydrophilic surface—with a polar solution. Although the surface of SiO_2 is naturally hydrophobic, it can be transformed to a hydrophilic one by the treatment with ultraviolet light, plasma, or chemical reagents [19, 20, 22]. Therefore, by controlling surface properties and selecting an appropriate solution, the patterning procedure can be performed more easily than the lithographic one, especially when combined with solution-based techniques such as spin coating, inkjet printing, and dip coating. To explore this possibility, the wetting properties of ISO films and their deposition on hydrophobic surfaces were investigated elsewhere [11].

In this study, ISO thin films and TFTs were fabricated for the first time on hydrophilic surfaces using polar solutions. The stabilization of their amorphous structures and improvement of device characteristics, such as the reduction of the absolute values of threshold voltage $|V_T|$ (to magnitudes near 0 V) and off current, were similar to those observed for the ISO TFTs manufactured by the sputtering method [10].

2. Experimental methods

The solution processing technique described by Han *et al* [22] was modified to make it applicable for the fabrication of ISO films. Precursor solutions for spin coating were prepared by dissolving indium chloride ($InCl_3$) powder (CAS: 10025-82-8) in acetonitrile (CH_3CN) solvent (CAS: 75-05-8) at a molar concentration of 0.05 M. Acetonitrile is a solvent with a low boiling point and high evaporation rate; hence, it evaporates relatively fast during spin coating, leading to the formation of non-uniform films. Therefore, a small amount of high boiling point ethylene glycol solvent ($HOCH_2CH_2OH$; CAS: 107-21-1) was added to the $InCl_3$ solution at an ethylene glycol to acetonitrile a volume ratio equal to 1/50. As a result, uniformly coated films were obtained despite fast evaporation of the acetonitrile because the presence of ethylene glycol species allowed $InCl_3$ molecules to spread across the substrate surface. In addition, it was found that increasing the concentration of ethylene glycol in solution produced more inhomogeneous films due to the solvent-induced dewetting. For this reason, the solution should contain a greater fraction of the low boiling point solvent and a much smaller fraction of the high boiling point solvent. Because of low solubility of $InCl_3$ to acetonitrile, the solution was subsequently stirred at room temperature for at least 1 week using a magnetic stirrer to reach high degrees of uniformness and consistency. For Si doping, tetraethyl orthosilicate (TEOS; CAS: 78-10-4) was added to the reaction solution with Si contents to In of 3, 5, 10, or 15 at%. TEOS containing slution was sttirred for a few hours and folowed by spin coating as shown bellow; long time stirring of TEOS containing solution resulted in degradation of the solution.

SiO_2 (250 nm)/Si (high doped p-type) wafers were used as the substrates. SiO_2 plays a role as a gate insulator. Because the obtained solution was polar, while the SiO_2 surface was hydrophobic, the substrate was sonicated in a 1 M sodium hydroxide (NaOH) solution for 5 min to attach hydrophilic OH groups to its surface and thus facilitate the coating process. After treatment, the prepared precursor solution was dropped on the substrate and rotated at a speed of 3000 rpm for 30 s. The obtained samples were dried at a temperature of 100 °C for 5 min, and the coating procedure was repeated again until a desired thickness was achieved. Finally, the produced specimens were annealed for 30 min in air at various temperatures ranging from 250 °C to 800 °C for structural characterization. Thicknesses, densities, roughness values, and crystallization temperatures of the obtained thin films were determined by x-ray reflectivity (XRR) and x-ray diffraction (XRD) techniques using a Rigaku Ultima IV system with Cu Kα ($\lambda = 1.540\,56$ Å) radiation and cross beam optics [23–25].

To fabricate a transistor, source and drain Al electrodes with thicknesses of 200 nm were deposited on the fabricated film surface by thermal evaporation through a stencil shadow mask with various channel sizes. The channel width was set to 1000 μm, whereas the channel length varied from 50 μm to 350 μm. Device characteristics of the manufactured TFTs including the output (drain current I_D versus drain-source voltage V_{DS}) and transfer (I_D versus gate-source voltage V_{GS}) ones were determined at room temperature and ambient pressure using a Keysight B2912A system.

All transfer characteristics were measured in the saturation regime because the produced TFTs were operated at high V_{DS} values corresponding to the saturated drain current. In this regime, the magnitude of I_D can

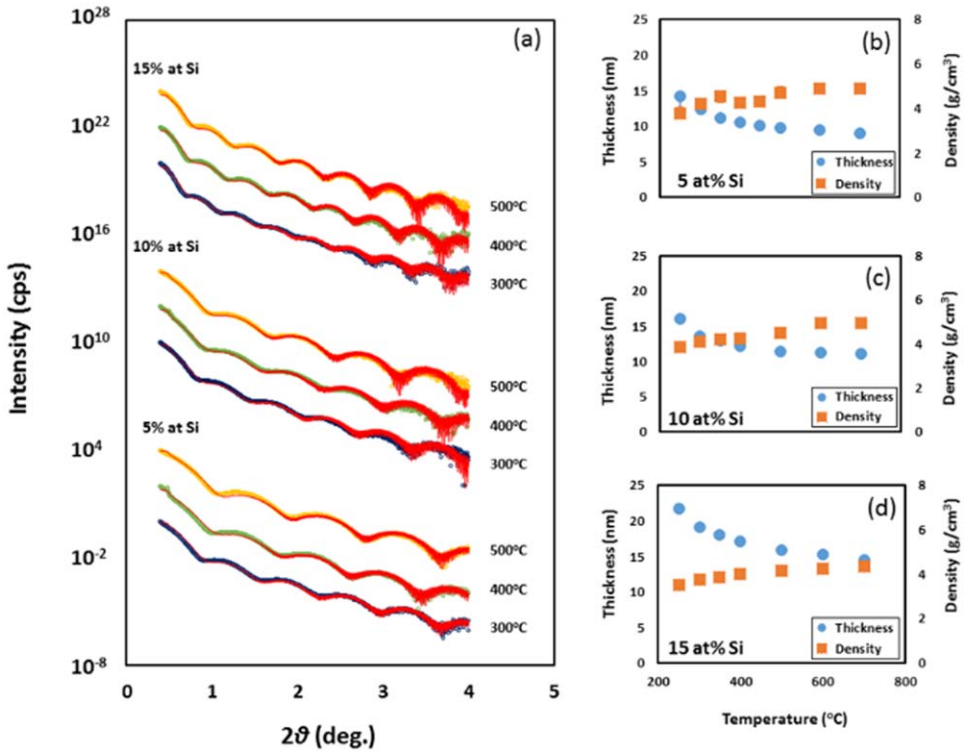

Figure 1. (a) XRR profiles of the ISO thin films with various concentrations of Si dopant. Their positions are aligned along the vertical direction for clarity. The experimental data points depicted by the blue, green, and orange circles were obtained for the thin films annealed at 300, 400, and 500 °C, respectively. The red curves denote the fitting data obtained with the GenX software. Using these results, film thicknesses (blue circles) and densities (orange squares) were estimated for the specimens containing (b) 5 at%, (c) 10 at%, and (d) 15 at% Si. The calculated error bars were relatively small.

be expressed as

$$I_{\mathrm{D}} = \frac{W.\mu.C_{\mathrm{i}}}{2L}(V_{\mathrm{GS}} - V_{\mathrm{T}})^2, \tag{1}$$

where μ is the field-effect mobility, C_{i} is the capacitance per unit area of the gate insulator, and V_{T} is the threshold voltage [26]. Hence, the field-effect mobility μ can be determined as follows:

$$\mu = \frac{2L}{W.C_{\mathrm{i}}}\left(\frac{\partial\sqrt{I_{\mathrm{D}}}}{\partial V_{\mathrm{GS}}}\right)^2. \tag{2}$$

After plotting $\sqrt{I_{\mathrm{D}}}$ versus V_{GS}, the magnitudes of μ and V_T were estimated from the slope and intercept of the fitting line, respectively [27].

3. Results and discussion

3.1. Effects of Si doping on the density, thickness, and crystallinity of ISO film

The XRR profiles obtained for the ISO films with Si contents of 5, 10, and 15 at% exhibit oscillations (see figure 1(a)), whose periods and amplitudes reflect their thicknesses and densities, respectively. Generally, surface roughness is related to the XRR intensity decay rate and the interface roughness is determined from the XRR oscillation decay rate at higher angles [24]. It is clear that increasing the annealing temperature increased the oscillation period.

The GenX software was used to estimate the thicknesses, densities, and roughness values of the produced films using the method described in the previous section [11, 28]. The obtained fitting data are displayed as the red curves in figure 1(a). In addition, density and thickness were plotted as functions of the annealing temperature at Si contents of 5, 10, and 15 at% in figures 1(b)–(d), respectively. As the annealing temperature increased to 400 °C, the residues present inside the film, such as organic functional groups of the raw materials and fragments of the organic solvent, evaporated [11], reducing the film thickness and increasing the film density. After the evaporation process was complete, the film thickness and density remained unchanged regardless of the further increase in the annealing temperature. The ideal densities of the bulk ISO specimens

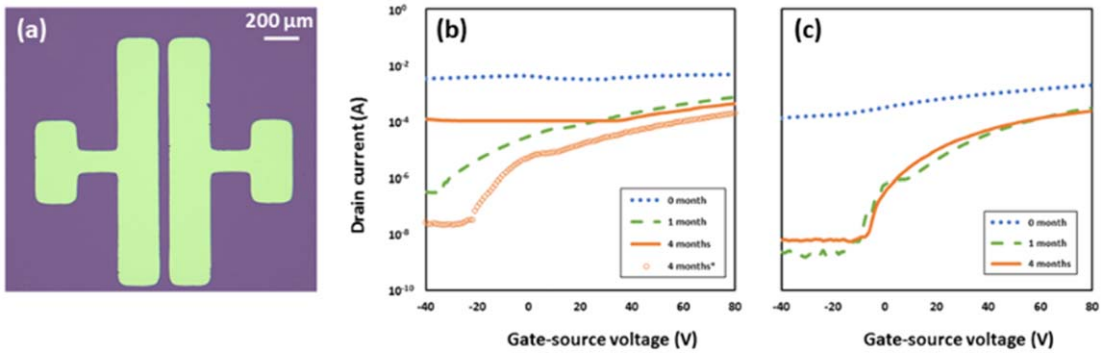

Figure 2. (a) The top view of ISO thin film at the $L = 50$ μm and $W = 1000$ μm. Transfer characteristics of the (b) IO TFT and (c) ISO (3 at% Si) TFT with $L = 50$ μm and $W = 1000$ μm annealed at 500 °C in air, which were recorded at $V_{DS} = 40$ V and various storage times, except for the orange circles in figure 2(b), which were obtained for the 4-month IO TFT at $V_{DS} = 100$ V as a reference.

with Si contents of 5, 10, and 15 at% were 6.9, 6.7, and 6.5 g cm^{-3}, respectively. However, as shown in the figures 1(b)–(d), the values estimated in this work were much smaller than the ideal ones. In addition, increasing the concentration of Si dopant increased the film thickness, which was consistent with the observed reduction in the film density. For instance, at an annealing temperature of 500 °C, the thicknesses of the films containing 5, 10, and 15 at% Si were around 10, 11, and 16 nm, while their densities were approximately 4.7, 4.5, and 4.1, respectively. This phenomenon can be attributed to the stabilization of the ISO amorphous structure by Si doping because stable amorphous materials typically contain networks with voids that decrease their densities [29].

The RMS roughness values of IO and ISO films estimated from XRR profiles increased with increases of Si concentration and annealing temperature, varing from 0.2 nm for as-deposited IO to 1.1 nm for ISO with 15 at% Si annealed at 1000 °C. For thin films used for TFTs annealed at 400 °C–600 °C (discussed in sections 3.2–3.5), the values are around 0.7 nm. Although they are larger than thsoe of ISO films fabricted by DC sputtering (ca. 0.23 nm) [6], surface roughness of ISO films fabricated by spin coating in this work was much smaller than thin-film thicness ($\gtrsim$10 nm), and was small enough for aplication to the channel of TFTs.

The crystallinity of the studied ISO films was examined by performing XRD measurements. It was found that in the temperature range of up to 800 °C, no crystalline phases were detected. In other words, the produced ISO thin films remained fully amorphous even at high annealing temperatures.

3.2. Effect of ageing on TFT characteristics

The top view of ISO thin film at $L = 50$ μm and $W = 1000$ μm was shown at figure 2(a), observed by an optical microscope BX53M. Figures 2 (b) and (c) illustrate the transfer characteristics of pure InO TFT (0 at% Si) and ISO TFT (3 at% Si) with the channel length $L = 50$ μm and channel width $W = 1000$ μm annealed at 500 °C in air, which were obtained at different storage times ranging from 0 month to 4 months. Although the IO TFT was conductive before storage and did not exhibit any conductance modulation by V_{GS}, the latter phenomenon was observed at a V_T of about −34 V after 1 month of storage. After 4 months of storage, the magnitude of V_T became very close to 0. However, after several measurements conducted under bias conditions, the TFT became conductive again, suggesting that the electronic properties of IO films were very unstable.

It is well known that in metal oxide semiconductors including In_2O_3, charge carriers are generated by the formation of oxygen vacancies [30]. Therefore, ideal In_2O_3 is a good semiconductor without defects; however, it can become very conductive due to the presence of charge carriers generated by oxygen defects, which was observed in this work for the 0-month IO TFT; the formation of these defects likely occurred during the thermal evaporation stage of the electrode deposition process conducted in high vacuum. As a result, the operation of the IO TFT was observed after 1 month of storage and continued after 4 months of storage suggesting that oxygen species penetrated the thin film and gradually filled its defects. Nonetheless, after several consequent measurements, the 4-month IO TFT ceased to be a semiconductor and reversed back to the conductive mode. This behavior might result from the release of oxygen under the bias conditions due to the small dissociation energy of the In−O bond [31]; various bond dissociation energies obtained for O and several other elements including In and Si are listed in table 1.

On the other hand, although the ISO TFT also exhibited conductive behavior immediately after electrode deposition, its conductance was modulated by V_{GS}. Conductance modulation became significant with an V_T of about −13 V after 1 month of storage and varied only slightly in the period between 1 month to 4 months. In both cases of IO and ISO TFTs, it can be suggested that the number of oxygen defects was reduced after storage.

Table 1. Dissociation energies of the bonds between various elements and oxygen. Adapted from Luo, CRC Handbook of Chemistry and Physics, 90th Edition [31].

	Bond dissociation energy (kJ mol^{-1})
Zn−O	⩽250
In−O	346
Ga−O	374
Sn−O	528
Si−O	799
C − O	1076

Table 2. Effect of storage time on the performance of TFTs annealed at 500 °C in air.

Sample	Threshold voltage V_T (V)	Mobility μ (cm^2/Vs)	Subthreshold swing (V/dec)	On/off current ratio
0-month IO TFT	—	conductive	—	—
1-month IO TFT	−34	0.80	14	2×10^3
4-month IO TFT	—	conductive	—	—
0-month ISO TFT	—	conductive	—	—
1-month ISO TFT	−13	0.58	5	2×10^5
4-month ISO TFT	−7	0.29	4	4×10^4

However, the ISO TFTs stored for more than one month demonstrated much better performance and were more stable than the IO TFTs, which was consistent with the results obtained for the ISO TFTs fabricated by DC sputtering due to the high dissociation energy of the Si−O bond [10], indicating that the IO TFT was less efficient in capturing oxygen during prolonged storage. The longer was the storage time, the higher was the amount of captured oxygen, and the lower was the number of oxygen vacancies, which shifted the value of V_T to a magnitude close to 0. In other words, the longer storage times contribute to the improvement of V_T and subthreshold voltage while affecting the mobility μ and on/off current ratio. Table 2 lists the device parameters obtained for both the IO and ISO TFTs. A detailed comparison between the performances of these two devices will be conducted in the next section.

3.3. Dependence of TFT characteristics on Si concentration

Figure 3 illustrates the transfer characteristics of the 1-month IO TFT (0 at% Si) and 1-month ISO TFT (3 at% Si) with the channel length $L = 50$ μm and channel width $W = 1000$ μm annealed at 500 °C in air, which were obtained at $V_{DS} = 40$ V. The ISO TFT exhibited a low off current less than 10^{-8} A, which was almost equal to the limit of the utilized measurement system. On the other hand, the off current of the IO TFT was higher than that of the ISO TFT by about two orders of magnitude. In addition, the V_T of the IO TFT (about −34 V) was shifted to a magnitude close to 0 V after Si doping. These results are consistent with the phenomenon observed for DC-sputtered samples in previous studies [6–10], suggesting that the effective doping of indium oxide with Si and related reduction of the number of oxygen defects, because oxygen defects produce electron carriers, which increased the off current and absolute value of V_T.

The output characteristics of the 1-month IO and 1-month ISO (3 at% Si) TFTs annealed at 500 °C in air are shown in figure 4. At low V_{DS} values, the magnitude of I_D increased almost linearly with a slightly concave feature, suggesting the existence of an injection barrier between the source electrodes and the channels of the IO and ISO thin films.

The estimated values of μ, V_T, on/off current ratio, and subthreshold swing obtained for the IO TFT were 0.80 cm^2 V^{-1}s^{-1}, −34 V, 2×10^3, and 14 V/dec, respectively (see table 2). For the solution-processed IO TFT fabricated by Kim *et al*, μ was 0.04 cm^2 V^{-1}s^{-1}, V_T was 42.6 V, the on/off current ratio was 10^4, and the subthreshold swing was 23.8 V/dec [32]. In another study, a μ of 6 cm^2 V^{-1}s^{-1} and on/off current ratio of 10^3 were obtained for an IO TFT fabricated by the spin coating method [33]. As of today, the best TFT performance corresponding to a μ of to 55.26 cm^2 V^{-1}s^{-1} and on/off current ratio of 10^7 was reported by the Han group [22].

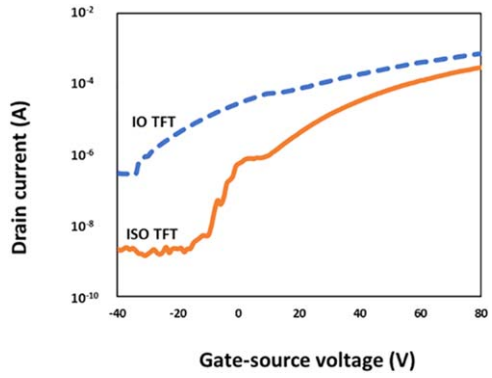

Figure 3. Transfer characteristic of the 1-month IO TFT and 1-month ISO (3 at% Si) TFT with $L = 50$ μm and $W = 1000$ μm annealed at 500 °C in air, which were obtained at $V_{DS} = 40$ V.

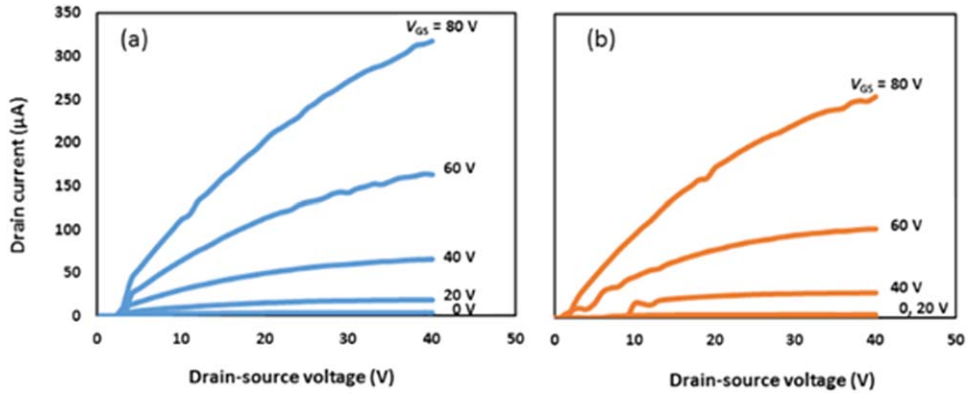

Figure 4. Output characteristic of the (a) 1-month IO TFT and (b) 1-month ISO (3 at% Si) TFT with $L = 50$ μm and $W = 1000$ μm annealed at 500 °C in air.

In contrast, the solution-processed ISO TFT exhibited significantly enhanced device characteristics as compared with those of the IO TFT fabricated in this work, except for the slight decrease in μ; the estimated values of μ, V_T, on/off current ratio, and subthreshold swing were 0.58 cm^2 V^{-1}s^{-1}, −13 V, 2 × 10^5, and 5 V/dec, respectively (table 2). Since the same behavior was observed for sputtered ISO TFTs in previous works [6–10], it can be concluded that Si doping reduced the number of oxygen defects and thus improved the magnitude of V_T. However, this process might also slightly reduce the value of μ.

3.4. Dependence of ISO TFT characteristics on annealing temperature

High annealing temperatures are unsuitable for solution processing since many substrates, such as glass and plastic ones, are unable to endure them. On the other hand, the results of thermal deposition spectroscopy studies [11] and dependence of the film density and thickness on the annealing temperature discussed in section 3.1 above (see figures 1(b)–(d)) suggest that organic contaminants can remain on the film surface at temperatures below 400 °C. Therefore, annealing temperatures of 400, 500, and 600 °C were selected for the TFTs fabricated in this study to remove contaminants from their surfaces as well as not too high temperatures.

Figure 5 displays the transfer characteristic of the 4-month ISO TFTs (3 at% Si) with the channel length $L = 50$ μm and channel width $W = 1000$ μm annealed at different temperatures between 400 °C and 600 °C in air, which were obtained at $V_{DS} = 40$ V. They show that the ISO thin films exhibit higher conductivity with increasing annealing temperature, which can be attributed to the larger number of oxygen defects; this trend is similar to the effects of ageing and Si concentration discussed in sections 3.2 and 3.3 respectively. Owing to the relatively small number of oxygen defects, the TFT annealed at 400 °C demonstrated the optimal performance corresponding to a small V_T of −5 V, low off current of about 10^{-10} A, small subthreshold swing of 2 V/dec, and high on/off current ratio of 10^5. Only $\mu = 0.04$ cm^2 V^{-1}s^{-1} was worse than that of the TFT annealed at 500 °C (0.07 cm^2 V^{-1}s^{-1}), which was likely caused by its relatively high carrier density in the on-state resulting from the presence of oxygen defects and applied V_{GS}. The device characteristics of the TFTs described in figure 5 are listed in table 3.

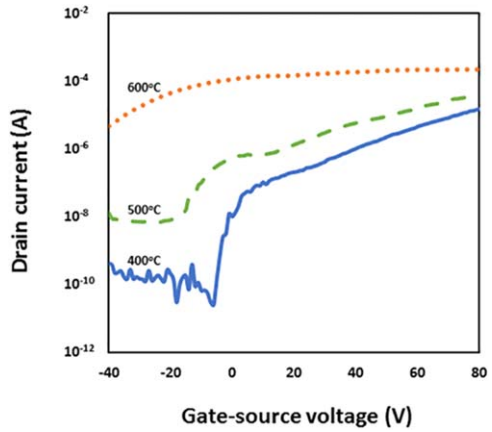

Figure 5. Transfer characteristics of the 4-month ISO (3 at% Si) TFT with $L = 50$ μm and $W = 1000$ μm annealed at various temperatures in air, which were obtained at $V_{DS} = 40$ V.

Table 3. Dependence of the device characteristics of the 4-month ISO TFTs on the annealing temperature.

Sample	Threshold voltage V_T (V)	Mobility μ (cm^2/Vs)	Subthreshold swing (V/dec)	On/off current ratio
400 °C ISO TFT	−5	0.04	2	10^5
500 °C ISO TFT	−15	0.07	6	3×10^3
600 °C ISO TFT	—	conductive	—	—

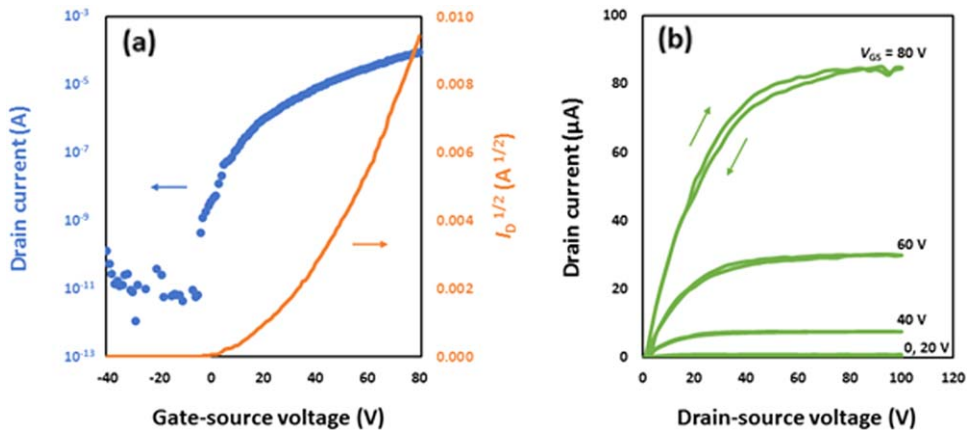

Figure 6. (a) Transfer characteristics at $V_{DS} = 100$ V and (b) output characteristics obtained for the 4-month ISO (3 at% Si) TFT with $L = 50$ μm and $W = 1000$ μm annealed at 400 °C in air.

3.5. Optimal performance of ISO TFTs

The results presented above revealed that the addition of a small amount of Si significantly improved the stability of the IO TFT system as well as the values of V_T, subthreshold voltage, and off current despite the slight decrease in μ. The optimal performance of the ISO TFTs was observed at low annealing temperatures and could be characterized by two sets of parameters. To obtain low values of subthreshold swing and V_T, small numbers of oxygen defects are preferred, while their large numbers are favorable for high values of μ. So far, to compare the parameters of the IO and ISO TFTs, their transfer characteristics were determined at $V_{DS} = 40$ V because the IO TFT was unstable under the high bias conditions described in section 3.2. However, to estimate the operation parameters of the ISO TFTs in the saturation regime more accurately, their transfer characteristics were determined at $V_{DS} = 100$ V to ensure that the drain current was fully saturated.

Figure 6 describes the transfer characteristics at $V_{DS} = 100$ V and output characteristics obtained for the 4-month ISO TFTs (3 at% Si) with the channel length $L = 50$ μm and channel width $W = 1000$ μm annealed at 400 °C in air. The estimated optimal values of μ, V_T, on/off current ratio, and subthreshold swing were 0.21 cm^2 V^{-1}s^{-1}, −5 V, 2×10^7, and 0.5 V/dec, respectively. Among the output characteristics, the forward

and reverse drain currents were almost identical, except for the curve obtained at a V_{GS} of 80 V. The hysteresis phenomenon might originate from the trap site near the interface between the channel and the gate insulator where the mobile carriers are confined at high applied V_{GS}.

As indicated by the results of other works on doped IO TFTs fabricated by spin coating [34], high values of μ are required for their satisfactory operation. Hence, further studies in this area will involve the use of different annealing environments (either containing oxygen gas or exposed to ultraviolet light in vacuum) and post-contact annealing procedures since they may enhance the performance of solution-processed metal oxide semiconductor TFTs at low temperatures [22, 35, 36]. Recent reports on detailed analysis of structure and electronic properties for other Si-doped oxides [37–39] will also help the improvement of device performance of ISO TFTs.

4. Conclusions

In this work, silicon-doped indium oxide thin films were prepared by the spin coating technique. The presence of Si atoms increased the stability of the In–Si–O amorphous structure at temperatures as high as 800 °C. With increasing the Si concentration, the film thickness increased as well, while the film density decreased. Furthermore, Si doping significantly decreased the absolute value of V_T of the ISO TFT and reduced its subthreshold voltage. The 3 at% Si-doped TFT annealed at 400 °C exhibited the smallest subthreshold swing of 0.5 V/dec, V_T of −5 V, μ of 0.21 $cm^2 V^{-1}s^{-1}$, and on/off current ratio of 2×10^7. In future, additional studies involving different annealing environments will be conducted to further improve the performance of solution-processed ISO TFTs.

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ORCID iDs

Toshihide Nabatame https://orcid.org/0000-0002-5973-0230
Akihiko Fujiwara https://orcid.org/0000-0002-1319-388X

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