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A Novel Independently Biased 3-Stack GaN HEMT Configuration for Efficient Design of Microwave Amplifiers

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Abstract: The power amplifier (PA) and low-noise amplifier (LNA) are the most critical components of transceiver systems including radar, mobile communications, satellite communications, etc. While the PA is the key component of the transmitter (TX), the LNA is the key component of the receiver (RX) of the transceiver system. It is pointed out that traditional design approaches for both the LNA and PA face challenging drawbacks. When designing an LNA, the power gain and noise figure of the LNA are difficult to improve simultaneously. For PA design, it indicates that efficiency and linearity of the PA are also hard to improve simultaneously. This study aims to surmount this by proposing a novel independently biased 3-stack GaN high-electron-mobility transistor (HEMT) configuration for efficient design of both PA and LNA for next generation wireless communication systems. By employing an independently biased technique, the proposed configuration can offer superior performance at both small-signal (SS) for LNA design and large-signal (LS) for PA design compared with other typical circuit configurations. Simulation results show that by utilizing an adaptive bias control of each transistor of the proposed configuration, both power gain and noise figure can be improved simultaneously for the LNA design. Moreover, efficiency and linearity can be also improved at the same time for the PA design. Compared results with other typical configurations including a single-stage, conventional cascode, independently biased cascode, and conventional 3-stack reveals that the proposed configuration exhibits superior advantages at both SS and LS operation.

Keywords: GaN HEMT; independently biased; microwave engineering; RF circuit design; low-noise amplifier; power amplifier

1. Introduction

The most critical requirements when designing an low-noise amplifier (LNA) include high power gain, low noise, and high reserve isolation, while these are high efficiency and high linearity when designing a PA. It has been shown that these requirements for both LNA and power amplifier (PA) are hardly to improve simultaneously. When designing LNA and PA, stacked circuit configurations are usually employed to enhance the circuit performance. Among the stacked configurations for design of the LNA and PA, cascode [1] and Darlington [2] configurations are two most important ones which can deliver various promising advantages over a single-stage configuration. The cascode configuration which offers high gain, high reverse isolation, and high frequency operation suits the design for both LNA [3–11] and PA [12–20] best, while the Darlington one, which offers high current gain, is highly suitable for PA design [21–25]. In the LNA design, it is generally pointed out that

noise and power gain are hardly to be improved at the same time. In [4,6,7] although the noise of the designed LNA can be reduced by employing an inductor which is added at the drain of the main transistor, the power gain of the resulting LNA is relatively low. On the other hand, [5] enhances the power gain of the LNA by using a forward bias and a capacitive divider but the noise figure is degraded accordingly. Additionally, it is obvious that the stacked configurations with more than three transistors are seldom developed for LNA design due to the significant increase of noise including shot noise and thermal noise caused by the added transistors. Besides LNA design, for the PA design two key parameters including efficiency and linearity are also hardly to be improved simultaneously. In [12,13] the efficiency of PA is enhanced by using a sliding bias technique and a new circuit topology, respectively. However, linearity is not mentioned in these articles implying that it is not considered. Although linearity is improved for cascode CMOS PA in [14,15] by employing an adaptive bias control and a pre-distorter, respectively, the efficiency of these PAs is poor. In addition to using the cascode and Darlington configurations for the design of the PA, recently stacked configurations have been also developed for this purpose [26–28]. In these articles, output power, power gain, and efficiency of the designed PAs are improved significantly at a very high operation frequency for both bipolar junction transistor (BJT)-type and field-effect transistor (FET)-type. Nevertheless, the two-tone linearity is still not considered for these stacked circuit configurations.

From these above considerations, this study aims to propose a novel stacked circuit topology which can be employed to improve critical performance of both LNA and PA simultaneously. It can be seen that one of the most serious issues of the mentioned stacked configurations, including the cascode, Darlington, and other typical stacked topologies, is that they have a floating potential at the connection points between two transistors. This means it is impossible to make operation of each transistor independent. This results in a degradation of performance of these circuits since operation condition of each transistor becomes inter-dependent. To surmount this, we propose an independently biased 3-stack GaN high-electron-mobility transistor (HEMT) configuration which is realized by connecting the traditional cascode circuit with an additional common-gate (CG) transistor. Moreover, two additional bias terminals are inserted at the floating points between transistors. The idea of the proposed topology is to keep the promising advantages of the cascode topology while making an adaptive control of bias condition for the 3 transistors.

Figure 1 illustrates how to realize such a circuit, along with other typical circuit configurations to be investigated. As can be seen in the figure, the independently biased 3-stack configuration is realized by connecting the independently biased cascode one with a third common-gate (CG) transistor. By inserting the two additional bias terminals, operation condition of the three transistors can be freely adjusted which cannot be done in conventional configurations. This helps to optimize both small-signal (SS) and large-signal (LS) characteristics effectively by adjusting bias condition of each individual transistor appropriately. Nevertheless, it is worth noting that if the number of transistor increases more, parasitic components will take effect seriously at higher frequencies limiting both SS and LS performance improvement. Although the advantages of such an independently biased technique have been investigated for GaAs HBT devices, including independently biased cascode and independently biased 3-stack in [29–32], the investigations for GaN HEMT devices have never been performed elsewhere. The rest of this paper is organized as follows. Section 2 investigates both the SS and LS characteristics of the proposed configuration in a comparison with other typical configurations. Section 3 will summarize and discuss the simulated results as well as give the future directions of the study.

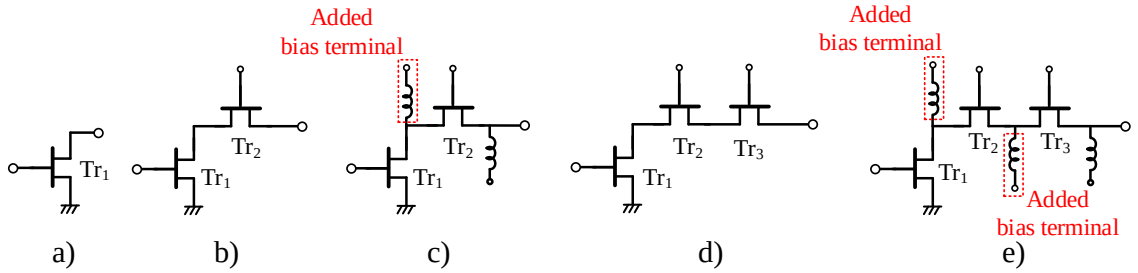

Figure 1. Circuit configurations: (**a**) single-stage; (**b**) conventional cascode; (**c**) independently biased cascode; (**d**) conventional 3-stack; (**e**) independently biased 3-stack.

2. Results

2.1. Small-Signal Investigation for LNA Design

In this section, key SS characteristics including power gain, noise figure, reverse isolation, and stability of the proposed configuration, which are critical for the design of LNA, are investigated in comparison with other typical configurations. These characteristics are evaluated through S-parameters of the configurations. The investigations are performed by employing an S-parameters analysis in a Keysight advanced design system (ADS) simulator [33]. The GaN HEMT SS models are provided by WIN Semiconductor Corp, Taoyuan City, Taiwan [34]. The schematics of the configurations are created inside the simulator. The simulation setup which is implemented in the Keysight ADS for S-parameters simulation is shown in Figure 2.

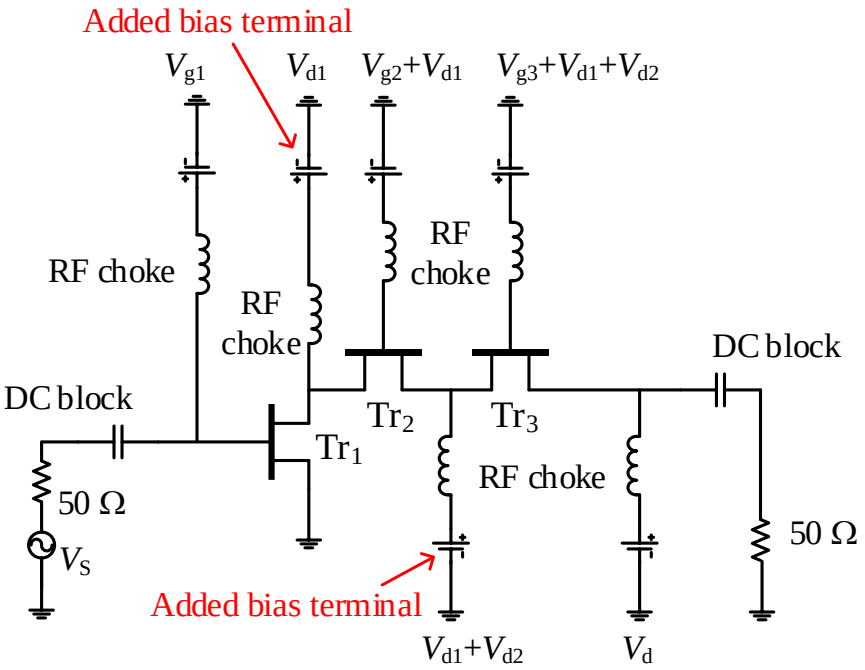

Figure 2. Simulation setup for S-parameters simulation in Keysight advanced design system (ADS).

Although the figure shows the simulation setup for the proposed 3-stack GaN HEMT configuration, the simulation setups for the other configurations are implemented in a similar way by placing a specific configuration to the schematic and connecting both its input and output to a same 50 Ω termination.

The high frequency small-signal equivalent circuit of the proposed 3-stack configuration shown in Figure 1e is illustrated in Figure 3 below. The equivalent circuit is realized by connecting the first SS equivalent circuit of the CS transistor and the second and third equivalent circuit of the CG transistors. It is worth noting that the gate-to-source conductance has been ignored in the figure because of its

negligible value. Here, v_1, v_2, v_3 and i_{d1}, i_{d2}, i_{d3} are gate-to-source voltages and drain currents of the first, second, and third transistor, respectively; g_{d1}, g_{d2}, g_{d3} and g_{m1}, g_{m2}, g_{m3} are drain conductance and transconductance of the first, second, and third transistor, respectively; C_{gs1}, C_{gs2}, g_{gs3} and C_{gd1}, C_{gd2}, g_{gd3} are parasitic gate-to-source and drain-to-gate capacitance of the first, second, and third transistor, respectively. This equivalent circuit will be used to derive critical SS parameters of the proposed configuration including reserve isolation, power gain, and stability.

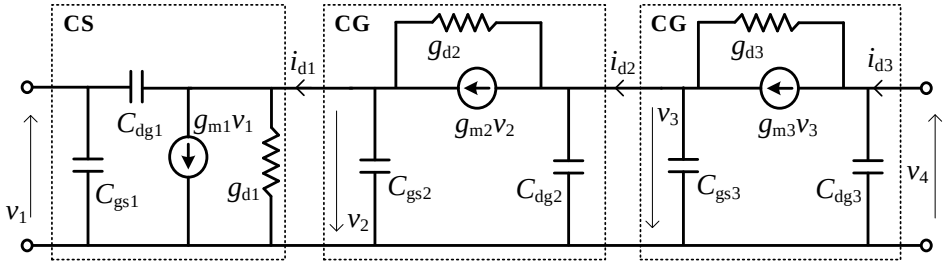

Figure 3. Small-signal equivalent circuit of the proposed 3-stack GaN high-electron-mobility transistor (HEMT) configuration.

This equivalent circuit will be used to derive critical SS parameters of the proposed configuration including reserve isolation, power gain, and stability. Firstly, regarding Figure 3, transmission (ABCD) matrix of the CS and CG transistors are derived as follows:

ABCD matrix of the CS transistor:

$$A_{\mathrm{CS}} \approx -\frac{g_d + j\omega C_{\mathrm{dg}}}{g_{\mathrm{m}}} \tag{1}$$

$$B_{\mathrm{CS}} \approx -\frac{1}{g_{\mathrm{m}}} \tag{2}$$

$$C_{\mathrm{CS}} \approx -\frac{j\omega C_{\mathrm{dg}}\left(g_{\mathrm{d}} + j\omega C_{\mathrm{gs}}\right) + g_{\mathrm{d}}\left(j\omega C_{\mathrm{gs}}\right)}{g_{\mathrm{m}}} \tag{3}$$

$$D_{\mathrm{CS}} \approx -\frac{j\omega C_{\mathrm{gs}}}{g_{\mathrm{m}}} \tag{4}$$

ABCD matrix of the CG transistor:

$$A_{\mathrm{CG}} \approx \frac{g_d + j\omega C_{\mathrm{dg}}}{g_{\mathrm{m}}} \tag{5}$$

$$B_{\mathrm{CG}} \approx \frac{1}{g_{\mathrm{m}}} \tag{6}$$

$$C_{\mathrm{CG}} \approx \frac{j\omega C_{\mathrm{dg}}\left(g_{\mathrm{m}} + j\omega C_{\mathrm{gs}}\right) + g_{\mathrm{d}}\left(j\omega C_{\mathrm{gs}}\right)}{g_{\mathrm{m}}} \tag{7}$$

$$D_{\mathrm{CG}} \approx \frac{-g_{\mathrm{m}} + j\omega C_{\mathrm{gs}}}{g_{\mathrm{m}}} \tag{8}$$

ABCD matrix of the configuration depicted in Figure 3 can be derived as below:

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} A_{\mathrm{CS1}} & B_{\mathrm{CS1}} \\ C_{\mathrm{CS1}} & D_{\mathrm{CS1}} \end{pmatrix} \begin{pmatrix} A_{\mathrm{CG2}} & B_{\mathrm{CG2}} \\ C_{\mathrm{CG2}} & D_{\mathrm{CG2}} \end{pmatrix} \begin{pmatrix} A_{\mathrm{CG3}} & B_{\mathrm{CG3}} \\ C_{\mathrm{CG3}} & D_{\mathrm{CG3}} \end{pmatrix} \tag{9}$$

From the above formula, the final ABCD matrix of the proposed configuration is given as follows:

$$A \approx \frac{j\omega C_{dg3}}{g_{m1}} \tag{10}$$

$$B \approx -\frac{1}{g_{m1}} \tag{11}$$

$$C \approx -\frac{\omega^2 C_{gs1} C_{dg3}}{g_{m1}} \tag{12}$$

$$D \approx -\frac{j\omega C_{gs1}}{g_{m1}} \tag{13}$$

Here, the following general approximations for MOSFET-type transistor are used: $g_m >> g_0$ and $g_m >> \omega C_{gs}$. These ABCD parameters are then converted to the S-parameters as below:

$$S_{11} = \frac{A + B/Z_0 - CZ_0 + D}{A + B/Z_0 + CZ_0 + D} \tag{14}$$

$$S_{12} = \frac{2\,(AD - BC)}{A + B/Z_0 + CZ_0 + D} \tag{15}$$

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D} \tag{16}$$

$$S_{22} = \frac{-A + B/Z_0 - CZ_0 + D}{A + B/Z_0 + CZ_0 + D} \tag{17}$$

In the following sections, the above S-parameters are used to derive critical SS parameters of the proposed configuration.

2.1.1. Reverse Isolation and Stability

Along with power gain and noise figure, reverse isolation and stability are very important parameters when designing the LNA. They are evaluated in term of scattering parameter S_{12} and μ criteria of a two-port network, respectively. Expression for S_{12} can be derived by using the formulas in the previous section:

$$S_{12} \approx \frac{2 g_{d1} g_{d2} g_{d3}}{g_{m1} g_{m2} g_{m3}} Z_0 j\omega C_{gs1} \tag{18}$$

From the above expression for S_{12}, it can be seen that the isolation of the proposed configuration is very high due to the triple contribution of the g_d/g_m with $g_m >> g_d$. Moreover, the expression also implies that S_{12} is dominated by the non-linear characteristic of C_{gs1}. This means that S_{12} of the LNA can be improved by adjusting the first gate bias voltage V_{g1}.

The μ criteria is a measure of stability and it indicates that if one two-port has larger μ, it is more stable. Moreover, if one two-port is stable, μ is greater than unity. Therefore, this criteria is usually used to compare stability among two-port networks. Here, μ is described through scattering parameters of a two-port network by the following formula [35]:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12} S_{21}|} \tag{19}$$

A two-port which has small S_{12} and high μ will be a great candidate for the LNA design. Thanks to the independently biased technique of the proposed 3-stack GaN HEMT topology, it is possible to adjust the bias condition of each transistor to improve both the reverse isolation and stability. Due to the fact that isolation of the proposed configuration is very high as mentioned earlier, $S_{12} = 0$ can be

assumed. Substituting the above derived S-parameters into this formula and using the approximations as mentioned in the last section and assumption $S_{12} = 0$, the expression of μ can be derived as below:

$$\mu \approx \frac{1}{|S_{22}|} \approx \left| \frac{1 - jZ_0\omega C_{gs1}}{1 + jZ_0\omega C_{gs1}} \right| \tag{20}$$

The above formula indicates that stability of the LNA is also dominated by the first gate bias voltage V_{g1} which contributes to the non-linear behavior of C_{gs1}. However, it is obvious that the effect of C_{gs1} on the stability is not significant due to the similar terms in both numerator and denominator.

From the above discussions, it can be concluded that V_{g1} is the dominant factor which mainly contributes to the improvement of both the isolation and stability of the LNA.

As mentioned, among the bias terminals including gate and drain bias terminals, the first gate bias (V_{g1}) plays a key role for the improvement of the isolation and stability. This is demonstrated in Figure 4, which shows the isolation and stability investigation with the variation of V_{g1} from -3.0 V to -1.0 V. As can be seen in the figure, isolation can be improved remarkably just by adjusting this bias terminal while the stability can be also slightly improved as expected. When V_{g1} decreases, not only can the S_{12} reach very low values below -40 dB in the entire frequency range, but the stability can be also improved.

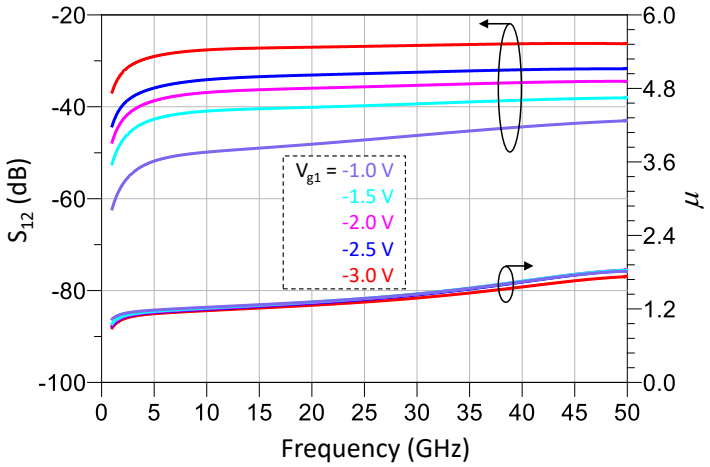

Figure 4. Power gain and noise figure characteristic of the proposed configuration.

2.1.2. Power Gain and Noise Figure

Power gain and noise figure (NF), which are expressed in terms of maximum available gain (MAG) and minimum noise figure (NFmin), respectively, are the most important parameters when designing LNA. Here, in order to compare power gain among the configurations, MAG is used and given by the following formula [35]:

$$\text{MAG} = \frac{S_{21}}{S_{12}} \left(K - \sqrt{K^2 - 1} \right) \tag{21}$$

where K is Rollett stability factor and is expressed through the scattering parameters as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}S_{21}|} \tag{22}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{23}$$

MAG in Equation (21) can be computed by using the expressions for S_{12} and S_{21} of the proposed configuration and using the general approximations as follows:

$$\mathrm{MAG} = \left(\frac{g_{m1}g_{m2}g_{m3}}{g_{d1}g_{d2}g_{d3}}\right)\left(\frac{g_{m1}}{\omega C_{gs1}}\right)\left(K - \sqrt{K^2-1}\right) \tag{24}$$

Equation (24) implies that the power gain of the proposed configuration is dominated by the first CS transistor due to the contribution of the term $g_{m1}/\omega C_{gs1}$. This once again confirms the fact that the first gate bias voltage V_{g1} is the critical bias parameter for improvement of isolation, stability, and power gain when designing an LNA. For the noise figure analysis, it is well known that noise of a cascaded system is always dominated by the first-stage or the first HEMT of the proposed configuration. This means the first gate bias voltage V_{g1} is the main factor contributing to the noise improvement. This is illustrated in Figure 5. The figure clearly shows that when V_{g1} varies from -3.0 V to -1.0 V, MAG, as well as NFmin, can change significantly. This means V_{g1} can be also utilized to improve both the MAG and NF. Once again, it can be seen that V_{g1} should be biased at low values to improve both the MAG and NF. Moreover, it is very interesting to see in the figure that both MAG and NF can be simultaneously improved for the proposed configuration when making an adaptive control of the V_{g1}.

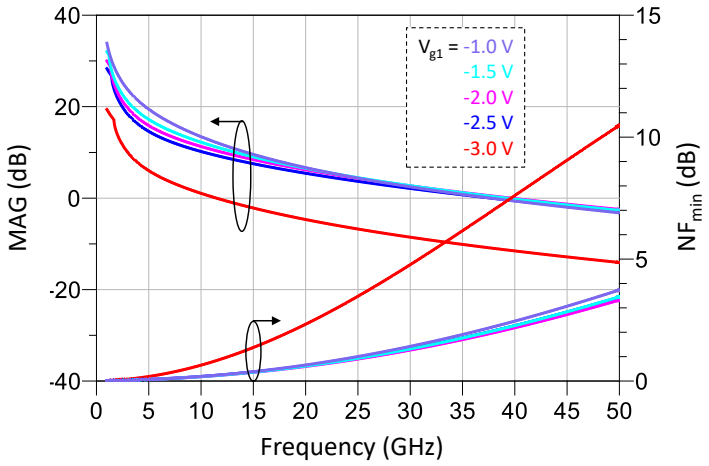

Figure 5. Reverse isolation and stability characteristic of the proposed configuration.

This is very important because as mentioned in the introductory section, MAG and NF are difficult to be improved simultaneously if using traditional design methods.

2.1.3. Comparison with Other Configurations

To further demonstrate advantages of using such a proposed 3-stack GaN HEMT configuration, its isolation, stability, power gain, and noise figure are compared with that of the other GaN HEMT configurations including a single-stage, conventional cascode, independently biased cascode, and independently biased 3-stack.

The bias conditions for all configurations are indicated in Table 1. It is worth noting that the configurations to be compared are biased at a class-A operation for the purpose of the SS investigation. In addition, for a fair comparison, the total drain bias voltage of 44 V and gate bias voltages of -2 V are kept similar for all configurations. As can be seen in the table, conventional configurations cannot adjust the bias condition independently for each transistor. Figure 6 shows the isolation comparison among five configurations. As analyzed before, SS critical parameters for designing LNA of the proposed configuration are mainly affected by the gate bias voltage of the first transistor.

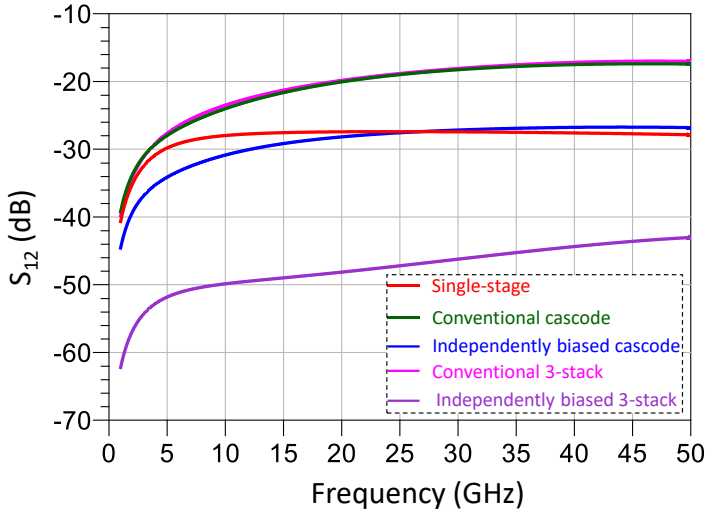

Figure 6. Reverse isolation comparison among configurations.

Table 1. Bias conditions of the configurations for small-signal (SS) investigations.

Configurations	V_{g1}	V_{g2}	V_{g3}	V_{d1}	V_{d2}	V_{d3}
Single-stage	−2 V	X	X	44 V	X	X
Conventional cascode	−2 V	−2 V	X	X	44 V	X
Independently biased cascode	−2 V	−2 V	−2 V	5 V	44 V	X
Conventional 3-stack	−2 V	−2 V	−2 V	X	X	44 V
Independently biased 3-stack	−2 V	−2 V	−2 V	1 V	3.5 V	44 V

By optimizing this bias voltage, the proposed 3-stack topology can achieve very low S_{12} compared with the other configurations. The isolation of the proposed configuration can reach below −40 dB in the entire frequency range from 1 GHz to 50 GHz. This very high isolation is excellent for the LNA design. Besides isolation comparison, Figures 7–9 show the comparison in stability, power gain and NF of the five configurations, respectively. Figure 7 indicates that the proposed configuration is more stable than the single-stage and independently biased cascode configurations in the entire frequency range. However, the conventional 3-stack and conventional cascode configurations are more stable than the proposed configuration below 25 GHz. The conventional configurations including conventional cascode and 3-stack are most stable compared with other ones. This is because they do not have additional feedback loops caused by the insertion of additional bias terminals as in the independently biased configurations. For the power gain comparison as shown in Figure 8, the proposed circuit exhibits superior MAG compared with other configurations below 2.5 GHz.

Nevertheless, at higher frequencies due to the parasitic elements, which occurs by adding the bias terminals, its MAG drops sharply. In general, the power gain of the proposed configuration can be better than the four configurations including conventional 3-stack, conventional cascode, and independently biased cascode. The single-stage has the highest MAG due to the lack of additional parasitic behaviour, while the conventional configurations have lowest MAG since they cannot adjust the operation conditions for each transistor. Finally, Figure 9 compares the NF among GaN HEMT configurations. Once again, it can be seen that conventional configurations, including cascode and 3-stack, have the poorest NF, while the other 3 configurations, including the proposed 3-stack, single-stage, and independently biased cascode, offer similar NF levels. However, at higher frequencies, the NF of the proposed configuration becomes worse due to its inherent parasitic behaviuor, as mentioned.

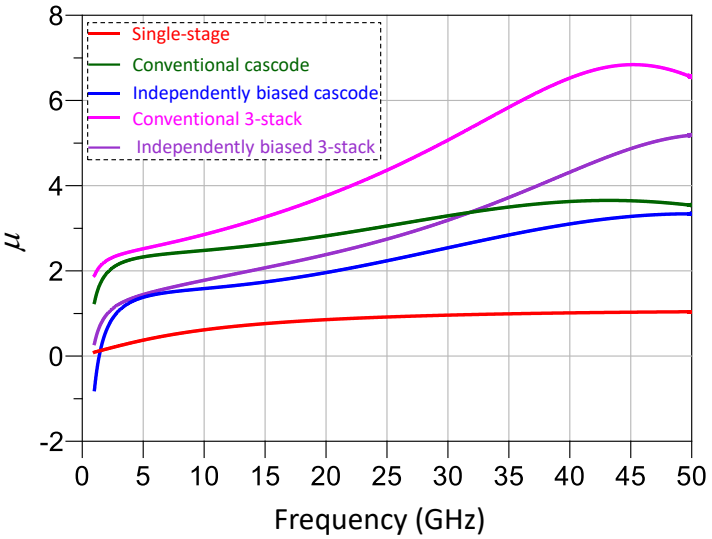

Figure 7. Stability comparison among configurations.

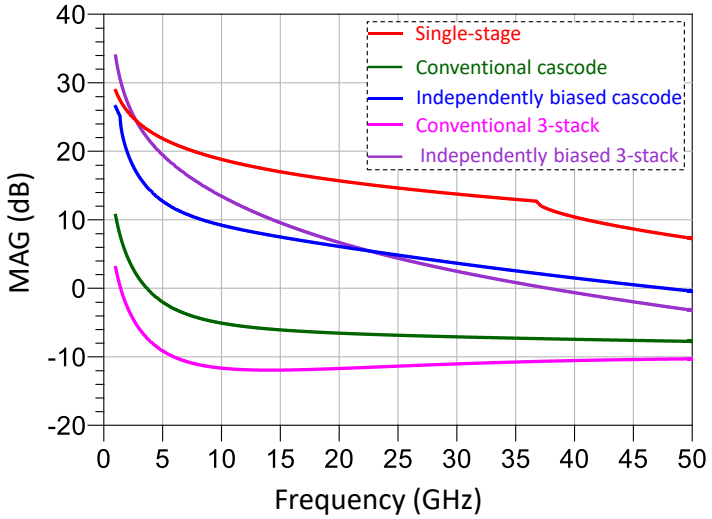

Figure 8. Power gain comparison among configurations.

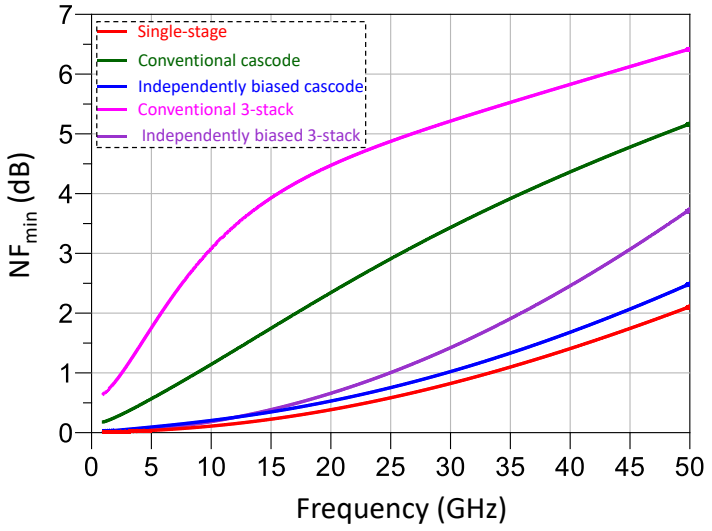

Figure 9. Noise figure comparison among configurations.

2.2. Large-Signal Investigation for PA Design

In this section LS performance including efficiency, linearity, output power, and power gain of the configurations are investigated. Here, efficiency is evaluated in terms of power added efficiency (PAE), while two-tone linearity is evaluated in term of third-order inter-modulation (IMD3). These are critical parameters when designing the PA. They are evaluated by using a Harmonic Balance analysis in the Keysight ADS simulator. The simulation setup implemented in the Keysight ADS for LS simulation of the configurations is similar to the one shown in the Figure 2 as for the SS performance investigation. The difference between the SS and LS simulation setup is that while port impedance in the SS simulation setup is set to 50 Ω, for the LS simulation it is set to Z_{Sopt} and Z_{Lopt} at the input and output, respectively. Here, Z_{Sopt} and Z_{Lopt} are optimum source and load impedance, respectively, and they are found by employing a source/load pull technique. In the Harmonic Balance analysis in the ADS simulator, a Krylov matrix solver type with a Krylov Restart length of 1000 is used. The convergence mode is set to Advanced with a maximum iterations of Robust. For the one-tone simulation of efficiency, power gain, and output power, 15 harmonics settings, which is high enough for the accuracy of the non-linear system, are used. For the two-tone simulation of the linearity (IMD3), 15 harmonics settings for each tone are also used.

2.2.1. Investigations

Figures 10–12 show the investigation of the linearity (IMD3) and efficiency (PAE) of the proposed configuration with respect to the variation of gate bias voltages V_{g1}, V_{g2}, and V_{g3}. As shown in the figures, V_{g1} contributes significantly to the change in both IMD3 and PAE, while V_{g2} only affects IMD3 at low-power region but it does not affect PAE; V_{g3} moderately affects IMD3 in the medium-power region and it affects PAE remarkably in the entire power range. This implies that both IMD3 and PAE can be simultaneously improved by adjusting the gate bias voltages. This is another very promising advantage of the proposed configuration because IMD3 and PAE are hard to improve simultaneously using traditional design methods, as mentioned in the introductory section.

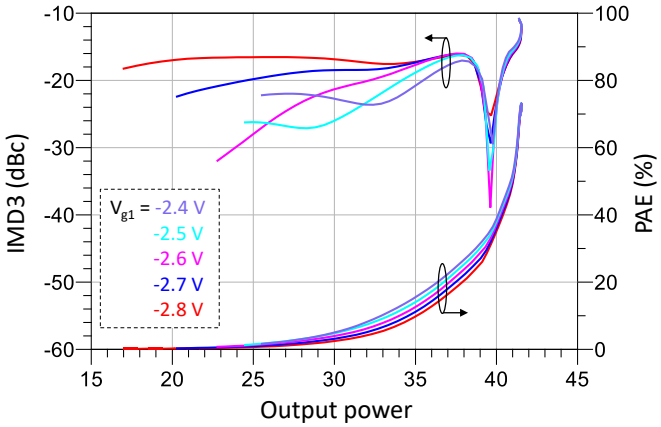

Figure 10. Large-signal (LS) investigation with V_{g1} variation.

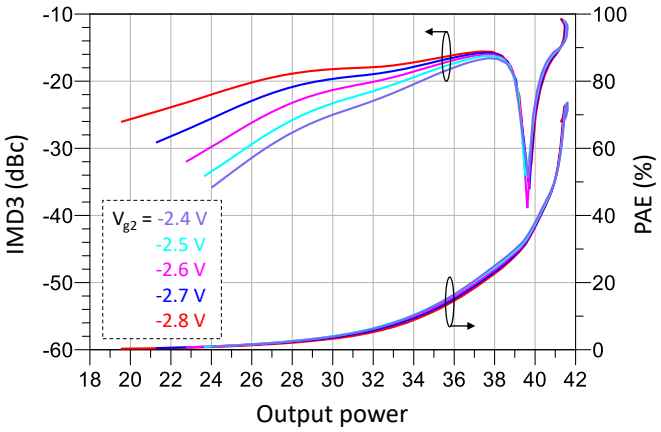

Figure 11. LS investigation with V_{g2} variation.

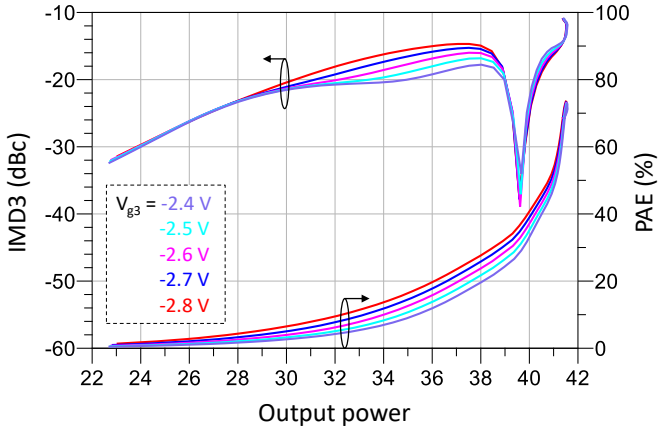

Figure 12. LS investigation with V_{g3} variation.

2.2.2. Comparison with Other Configurations

In order for an appropriate comparison of the LS operation, the bias conditions of each transistor of the independently biased configurations, including independently biased cascode and independently biased 3-stack, are individually optimized to achieve their best performance. The conventional configurations including single-stage, conventional cascode, and conventional 3-stack cannot do this due to the lack of the additional bias terminals. The LS investigation is conducted at an operation frequency of 3.5 GHz which is useful for using in next-generation of wireless communication systems. The GaN HEMT LS model is provided by WIN Semiconductor Corp. Figure 13 shows the comparison in output power and power gain among the configurations. Obviously, single-stage and cascode configurations have significantly low power gain and output power compared with that of the 3-stack configurations. The proposed 3-stack configuration has similar output power and power gain as that of the conventional 3-stack one. Both of them have the highest output power and power gain compared with the other configurations. This is because the 3-stack configurations can deliver higher output voltage swing.

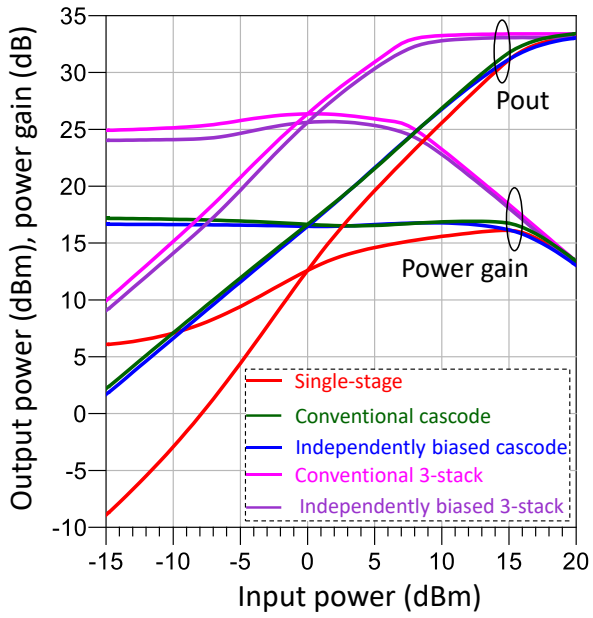

Figure 13. Output power and power gain characteristic.

It is noted that the efficiency of each configuration is obtained by using a load/source pull technique based on the LS GaN HEMT model to find out their optimum load/source impedances as mentioned previously. These optimum impedances for each configuration are given in Table 2.

Table 2. Optimum source and load impedances of the compared configurations.

Configurations	Source Impedance (Ω)	Load Impedance (Ω)
Single-stage	22.3 + j31.2	233 + j273
Conventional cascode	56 + j293	223.2 + j250
Independently biased cascode	56 + j293	223.2 + j250
Conventional 3-stack	55.9 + j101	179 + j273
Independently biased 3-stack	55.9 + j101	179 + j273

Additionally, the bias conditions of each configuration are given in Table 3. In contrast to the SS investigation in which operation condition is set at the class-A, in LS investigation the operation conditions of the transistor are set at a class-AB for the non-linear operation. Along with efficiency, another key performance when designing power amplifier is the linearity.

Table 3. Bias condition of configurations for large-signal (LS) investigation.

Configurations	V_{g1}	V_{g2}	V_{g3}	V_{d1}	V_{d2}	V_{d3}
Single-stage	−2.6 V	X	X	44 V	X	X
Conventional cascode	−2.6 V	−2.6V	X	44 V	X	X
Independently biased cascode	−2.6 V	−2.6 V	X	6 V	44 V	X
Conventional 3-stack	−2.6V	−2.6 V	−2.6 V	X	X	44 V
Independently biased 3-stack	−2.6 V	−2.6 V	−2.6 V	5 V	4 V	44 V

Although both the 3-stack configurations have similar output power and power gain, the efficiency of the conventional 3-stack one is poorer than that of the proposed 3-stack one, as indicated in Figure 14. As shown in the figure, the proposed 3-stack has superior efficiency among the configurations.In this paper, IMD3 is tested at a center frequency of 3.5 GHz with a frequency spacing of 4 MHz. In Figure 15 the IMD3 performances of the configurations corresponding to their efficiency are shown.

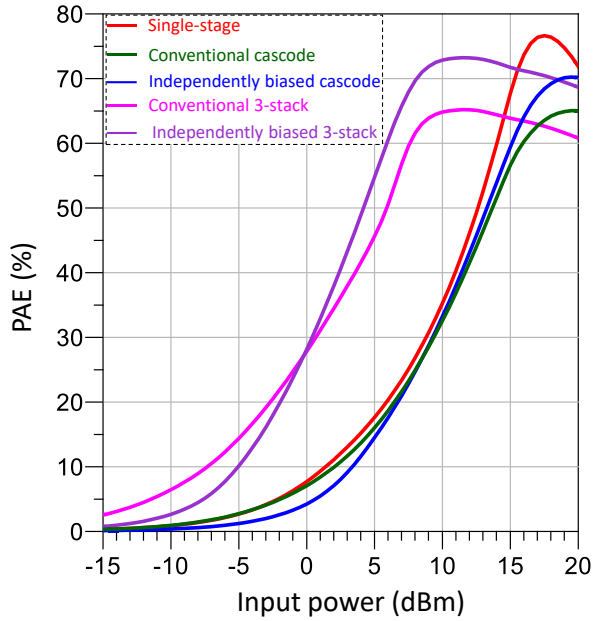

Figure 14. Efficiency characteristic.

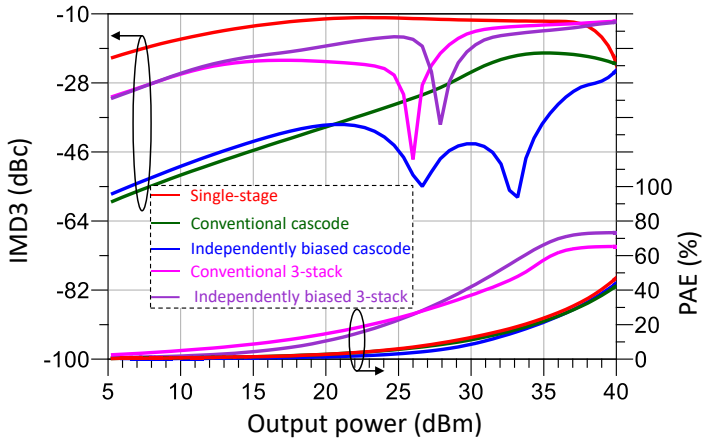

Figure 15. Linearity (IMD3) characteristic.

In IMD3 test, the limit level should be at −35 dBc. The figure shows that IMD3 of the single-stage cannot reach this level because it does not use any linearity improvement method. On the other hand, the other configurations can reach this IMD3 level. Table 4 summarizes this comparison. It can be seen in the table that at an IMD3 level of −35 dBc, the proposed 3-stack configuration has highest efficiency of 35% compared with that of the other configurations, by controlling the gate bias voltages. This verifies the advantage of the proposed configuration in term of both efficiency and linearity improvement.

Table 4. Summary of linearity and efficiency performance.

Configurations	IMD3 Level	PAE
Single-stage	−35 dBc	X
Conventional cascode	−35 dBc	4.5%
Independently biased cascode	−35 dBc	22.8%
Conventional 3-stack	−35 dBc	25%
Independently biased 3-stack	−35 dBc	35%

Finally, to demonstrate the advantage of such a proposed independently biased 3-stack circuit structure in terms of bandwidth, the PAE bandwidths of the 5 circuit configurations are compared to each other, as shown in Figure 16 below.

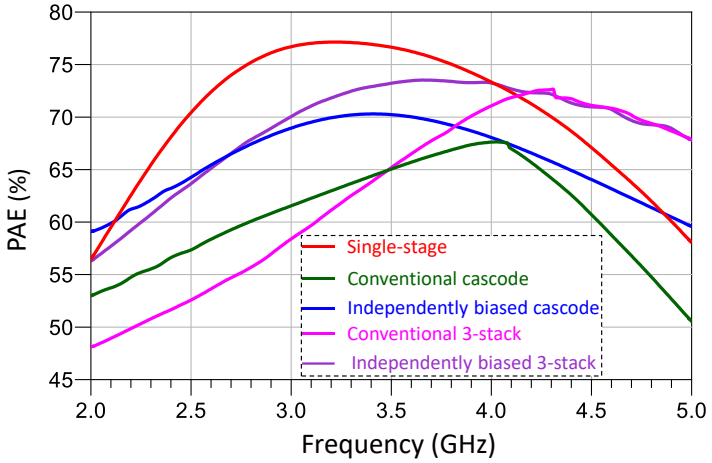

Figure 16. Power added efficiency (PAE) bandwidth comparison among configurations.

It can be clearly seen in the figure that the proposed 3-stack configuration exhibits superior PAE bandwidth over the others. The PAEs of the single-stage and independently biased casocode configurations drop significantly at both lower and upper frequency regions, while the PAEs of the conventional cascode and conventional 3-stack configurations are severely reduced in both the regions compared with other ones. The proposed configuration can maintain high efficiency in a wide frequency range compared with the other methods.

3. Discussion

This study has proposed a novel independently biased 3-stack GaN HEMT configuration to overcome inherent drawbacks of traditional design methods for both the LNA and PA of tranceiver systems. For the design of the LNA, the proposed configuration becomes an excellent candidate since it exhibits superior stability, isolation, power gain, and noise figure compared with other configurations. Both the power gain and noise figure can be simultaneously improved by an adaptive control of the gate bias voltage of the first transistor. Despite having a slight degradation of power gain and noise figure compared with that of the single-stage and independently biased cascode configurations at the high-frequency region, it still exhibits the best compromise of overall performance. For the design of the PA at an operation frequency of 3.5 GHz, it shows simultaneous improvement of efficiency and linearity by appropriately controlling the gate bias voltages of the individual transistors. The LS performance of the proposed configuration has been compared to that of the other configurations. The compared results indicate that the proposed topology offers the best compromise in efficiency and linearity improvement. Despite having poorer linearity than the independently biased cascode configuration, the proposed topology can deliver better efficiency at the same linearity level. Generally, although the independently biased cascode configuration has the similar ability of independent control of bias condition for each transistor, it cannot efficiently optimize both the SS and LS performance at the same time compared with the proposed configuration. Therefore, the proposed configuration becomes the best choice among the configurations for use in modern wireless communication systems.

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